

Compal Confidential

L360

M/B Schematic Document

AMD Cezanne Processor with DDR4 SO- DIMM

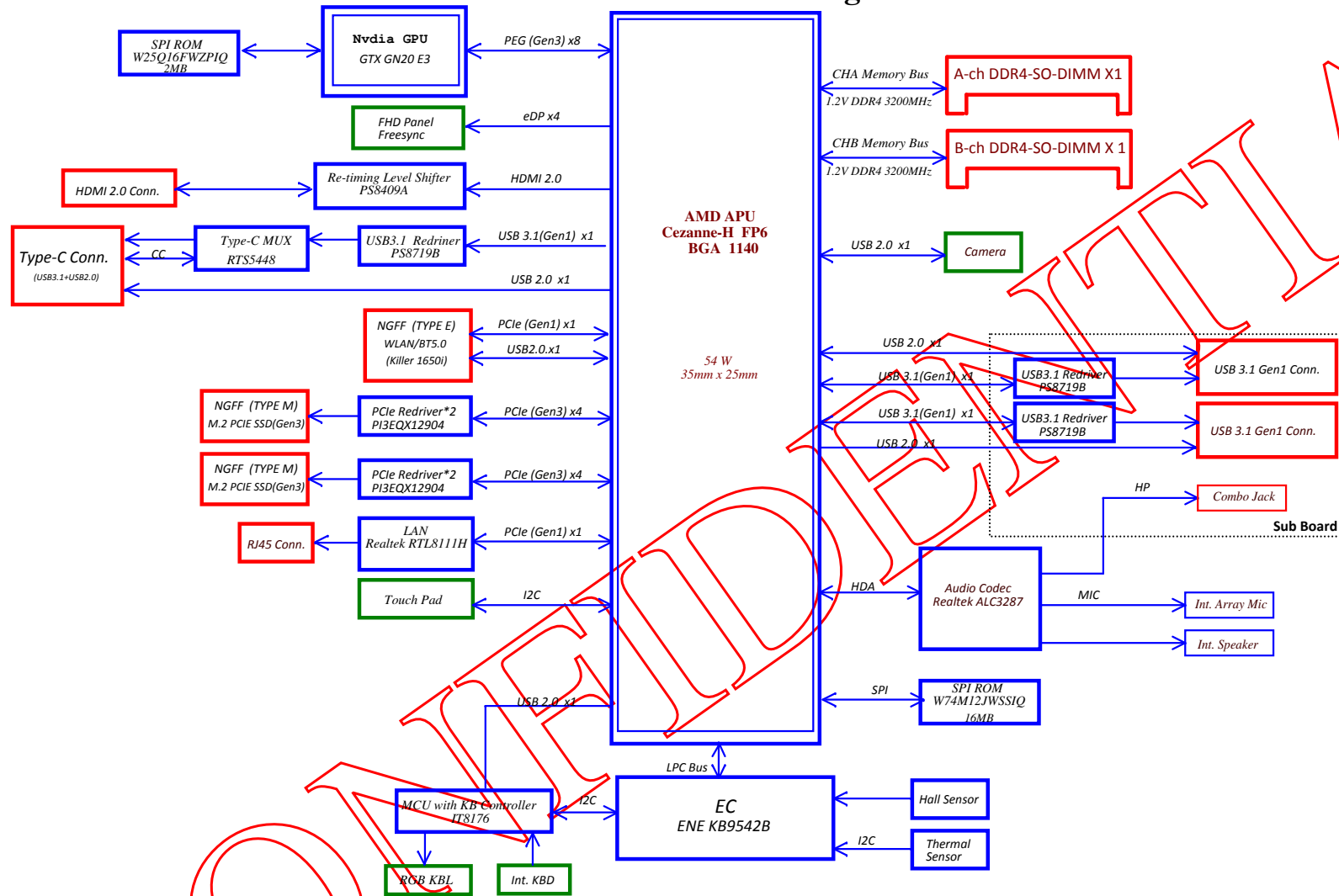
2020-08-17

LA-K971P

REV:0.2

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Issued Date	2019/12/03	Deciphered Date	2021/12/03	Title	Cover Page
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Cezanne-H Block Diagram



Voltage Rails

power plane				
State	+12. 6VB	+5VALW +3VALW +1. 8VALW +0. 75VALW	+1. 2V +2. 5V	+5VS +3VS +1. 8VS +0. 75VS +0. 6VS +APU_CORE +APU_CORE_SOC
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

BOM Structure Table

Item	BCM Structure
Memory Down - SDP Package	SDP@
Memory Down - DDP Package	SDP_CHB@
	DDP@
	DDP_CHB@
Channel B Memory Down	CHB@
EMI pop	EMI@
EMI un-pop	@EMI@
ESD pop	ESD@
ESD un-pop	@ESD@
RF pop	RF@
RF un-pop	@RF@
Debug	HDT@
Keyboard BackLight	KBL@
Normal FP	FP@
SLIM_FP	SLIM_FP@
CAMERA POWER CIRCUIT	CAM@
Modern standby	MS@
	NON_MS@
DP Power Switch	DPS1155@
	DPS1113@

USB 2.0 Port Table

Port	External USB Port
0	USB3.1 Type-C
1	USB3.1 Type-A
2	Camera
3	WLAN_BT
4	
5	USB3.1 Type-A
6	IT8176
7	IT8295

DDI Port Table

Port	Lane
0	eDP
1	HDMI
2	
3	

USB 3.0 Port Table

Port	External USB Port
0	USB3.1 Type-C
1	USB3.1 Type-A
4	
5	USB3.1 Type-A

GPP Port Table

Port	Lane	
0	0	LAN
1	1	WLAN
2	2	
3	3	
4	4	
5	5	JSSD1
6	6	
7	7	
8	8	
9	9	JSSD2
10	10	
11	11	

EC SM Bus1 address

EC SM Bus2 address

EC SM Bus4 address

Device	Address	Device	Address	IT8176FN	????
Smart Battery	????	Thermal Sensor (F75303M)	1001_101xb		
Charger (ISL89739A)	0x12				

PCH SM Bus address

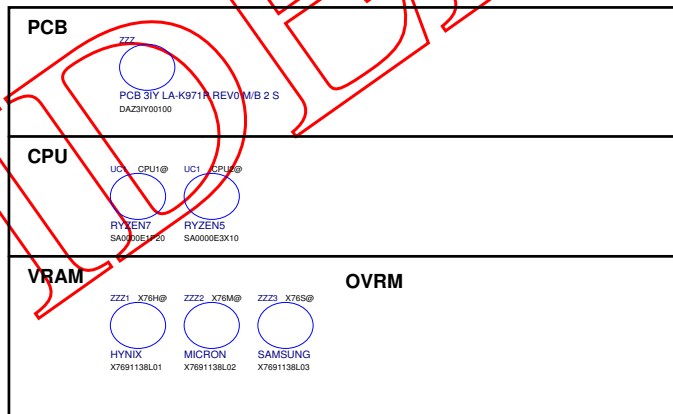
Device	Address	Device	Address
Touch pad			

Device	EC Bus	Slave Address (8 bit)
Battery	1	0x16
Charge	1	0x12
APU	2	0x78
APU Thermal sensor	2	0x98
Thermal sensor	2	0x9A
IT8176	4	0xCC
GPU	2	0x9E

SMBUS Control Table

	SOURCE	APU	BATT	CHARGER	KB9022	GPU	Thermal Sensor	IT8176FN
EC_SMB_CK1	KB9022	X	V	V	V	X	X	X
EC_SMB_DA1	+3VL		+3VALW	+19V_VIN				
EC_SMB_CK2	KB9022	V	X	X	V	V	V	X
EC_SMB_DA2	+3VS	+3VS			+3VS	+3VS	+3VS	
EC_SMB_CK4	X	X	X	X	X	X	X	V
EC_SMB_DA4								+3VALW_AG

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF



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Power Sequence

Boot

Shut
Down

EC Pin 110 Input

EC Pin 112 Output

AC Plug

EC Pin 114 Input

EC Pin 100 Output

EC Pin 122 Output

EC Pin 123 Input

EC Pin 6 Input

EC Pin 95 Output

EC Pin 116 Output

EC Pin 99 Output

EC Pin 121 Output

EC Pin 36 Input

EC Pin 32 Output

EC Pin 13 Input

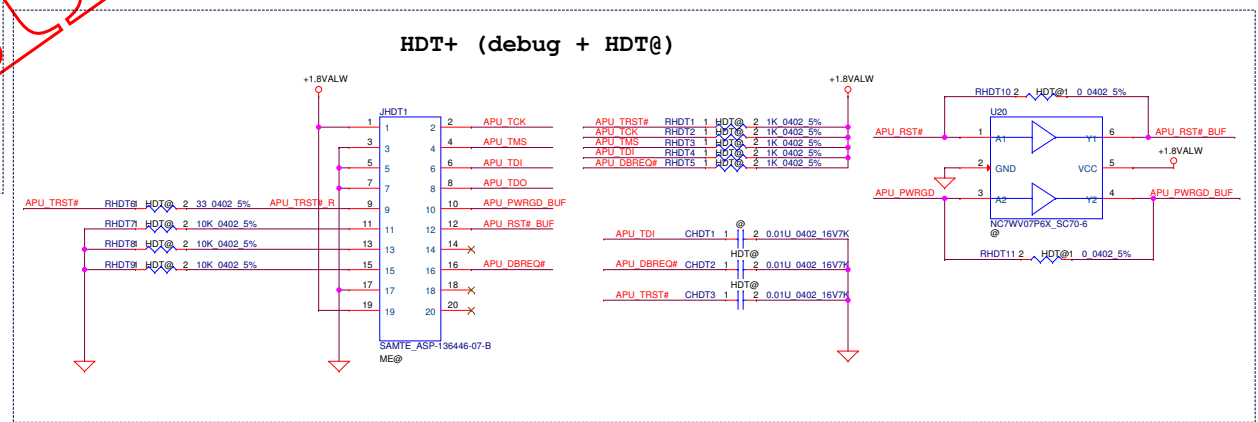
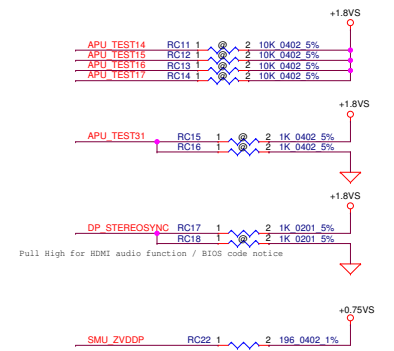


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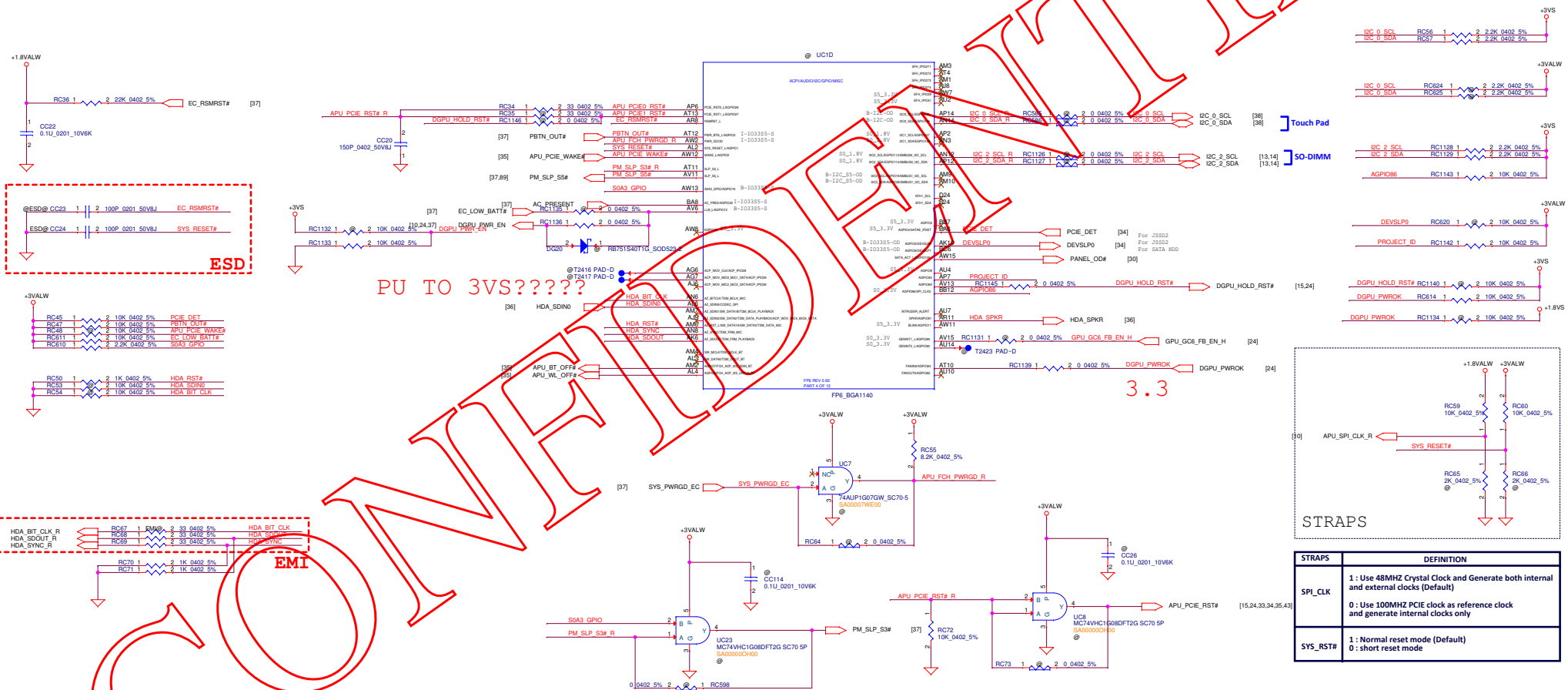


Main Func = CPU



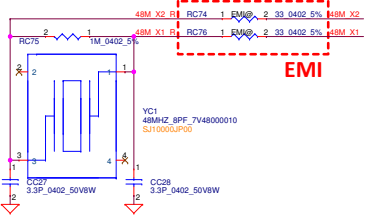


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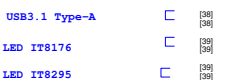
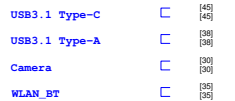
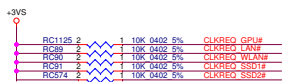
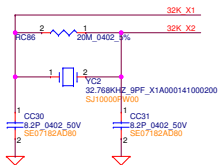


STRAPS	DEFINITION
SPI_CLK	1 : Use 48MHZ Crystal Clock and Generate both internal and external clocks (Default) 0 : Use 100MHZ PCIE clock as reference clock and generate internal clocks only
SYS_RST#	1 : Normal reset mode (Default) 0 : short reset mode

48MHz CRYSTAL



32.768KHZ CRYSTAL



1.8V

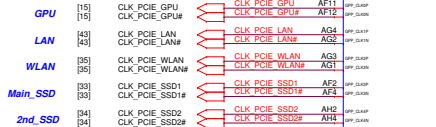
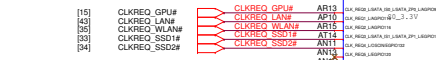
[9,24,37] DGPIU_PWR_EN

RC144 1 10 0.0402 5%

USB_OC#

RC288 1 2 100K 0.402 5%

USB_OC#



@ UC1J

USB

FPC_BGA1140

PART 10 OF 13

TYPE-C

Type-A M/B

Type-A SUB board

TYPE-C

Type-A M/B

Type-A SUB board

TYPE-C

Type-A M/B

Type-A SUB board

TYPE-C

Type-A M/B

Type-A SUB board

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@ UC1E

CLKREQ GPU#

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CLKREQ WLAN#

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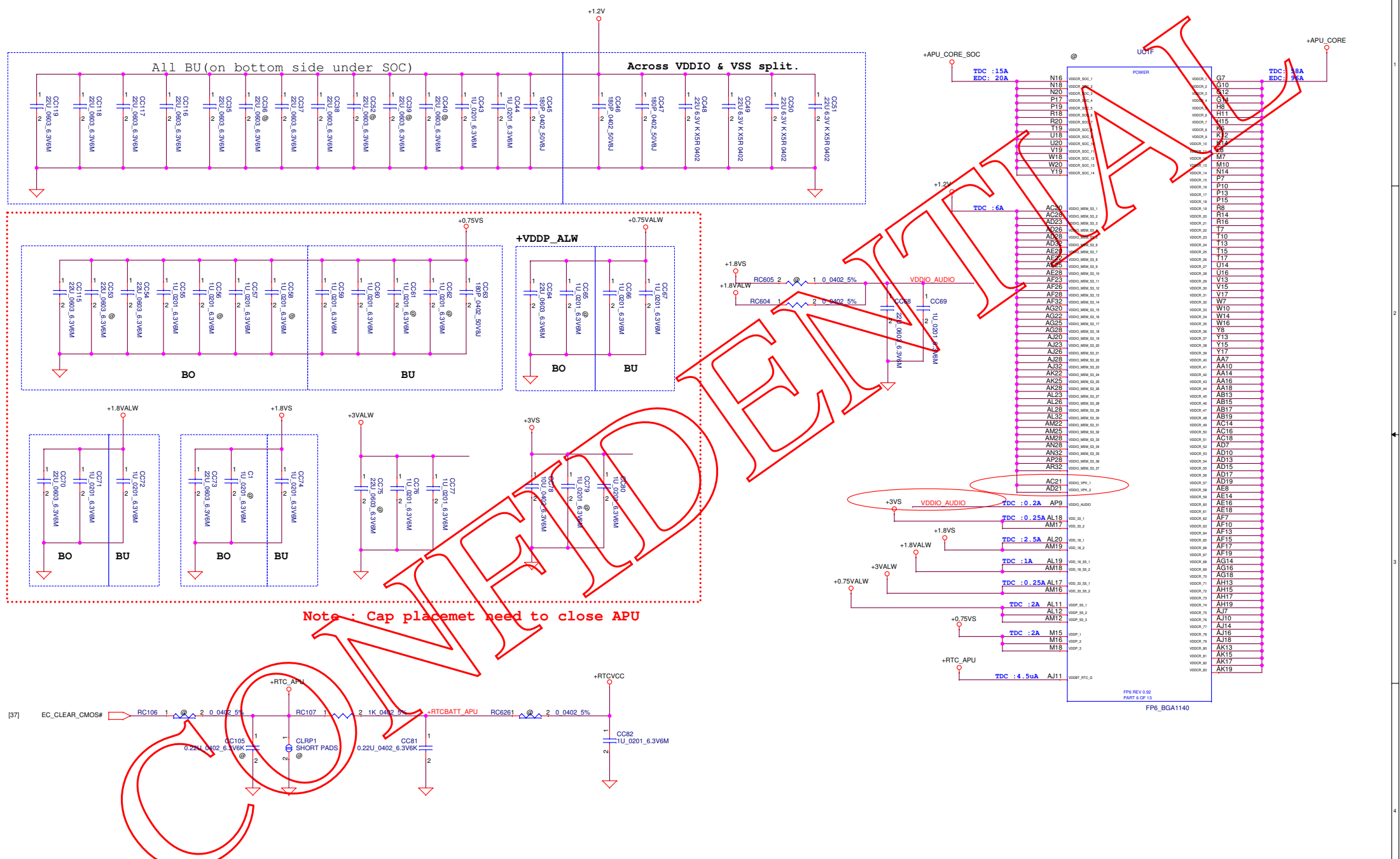
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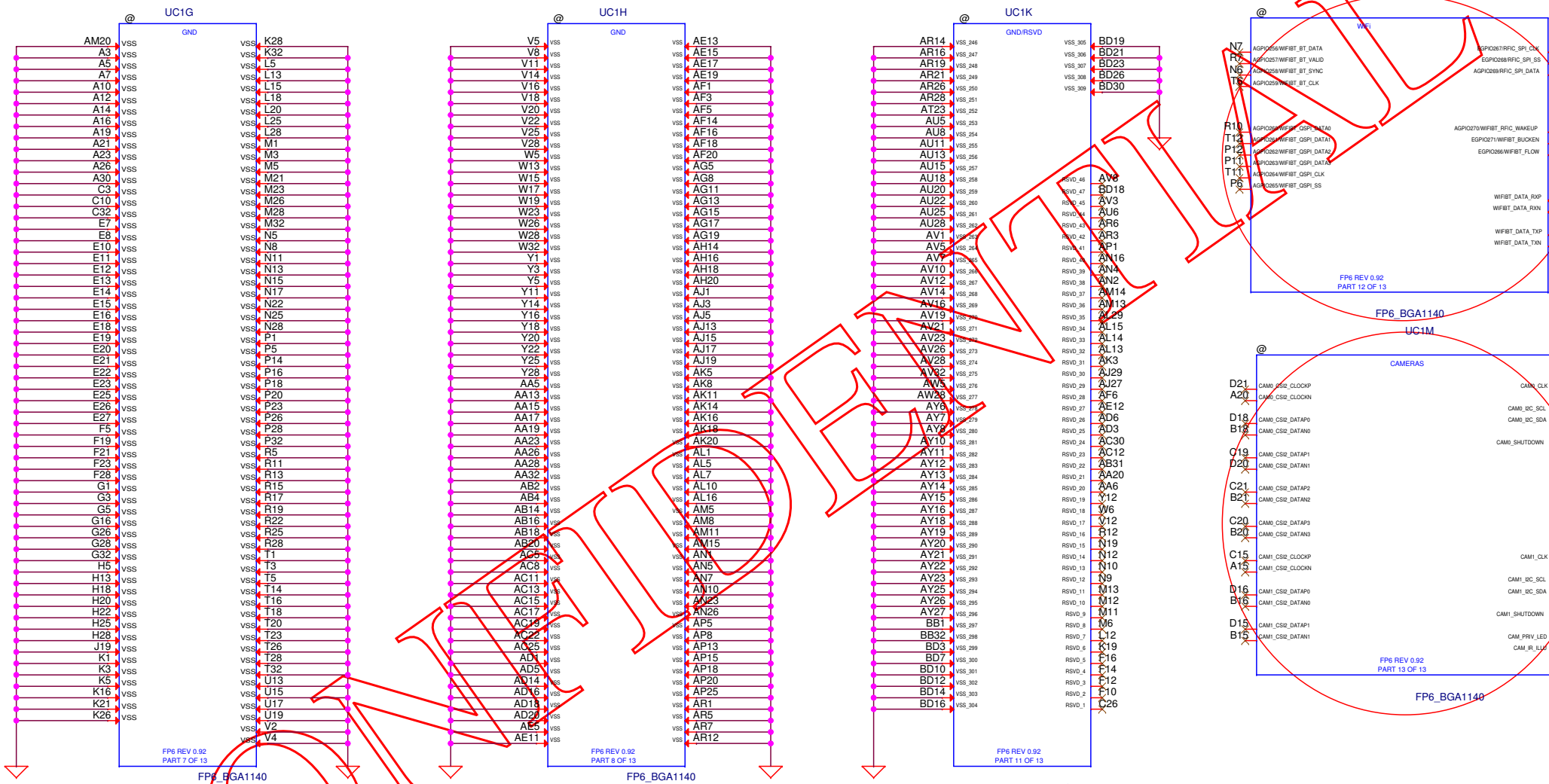
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Main Func = CPU



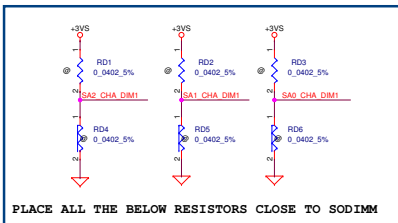
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Main Func = CPU



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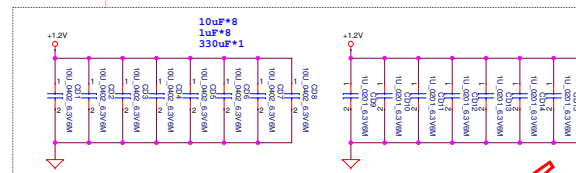
CHANNEL-A



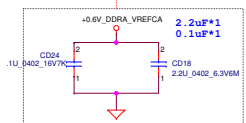
SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS:
READ ADDRESS:
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

(4.0 mm)

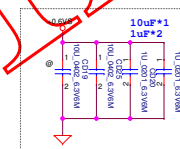
Layout Note:
Place near JDIMM2



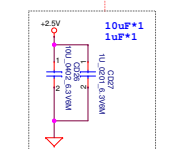
Layout Note:
PLACE THE CAP WITHIN 200 MILS
FROM THE JDIMM2



Layout Note:
Place near JDIMM2

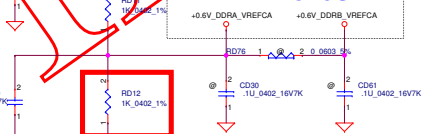


Layout Note:
Place near JDIMM2



PLACE NEAR TO PIN

DIMM Side

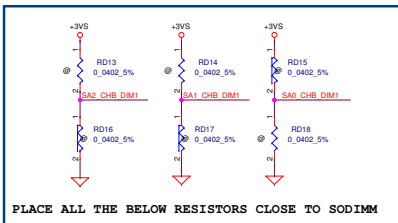


1.5K for ES DDR issue / 1K for QS sample
VREF traces should be at least 20mils wide
20mils spacing to other signals

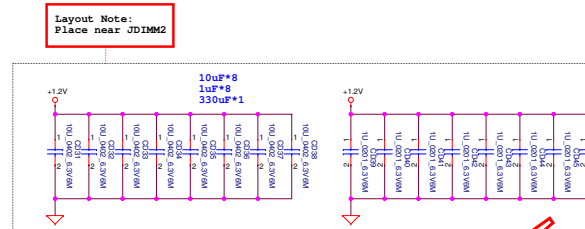
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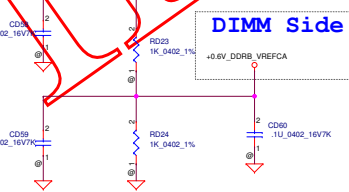
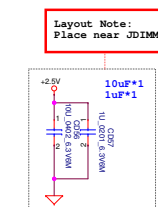
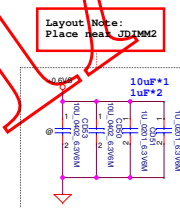
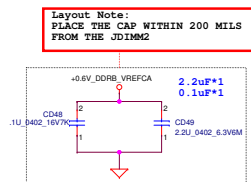
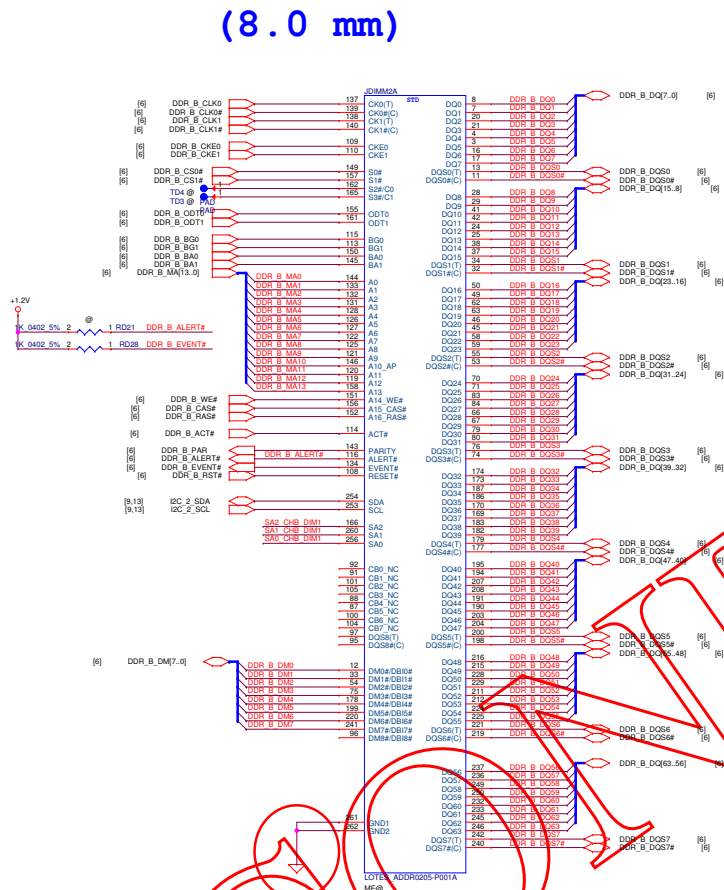
CHANNEL-B



```
SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS:
READ ADDRESS:
SA0 = 1; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S
```



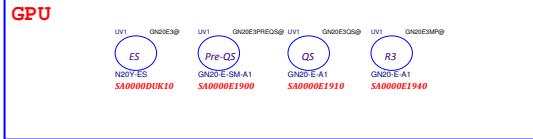
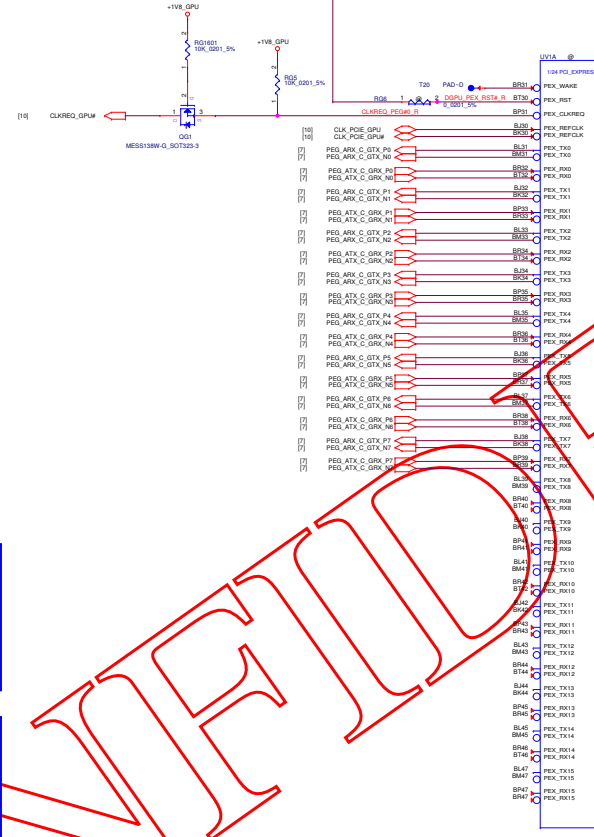
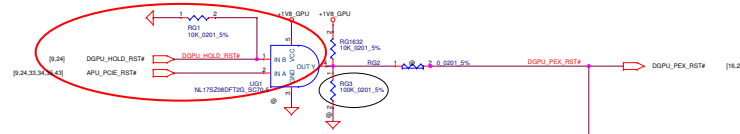
(8.0 mm)



STANDARD

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				Date	Thursday, February 24, 2021 14:01

GC OFF 1.0 GPU Power ON/OFF



Under GPU

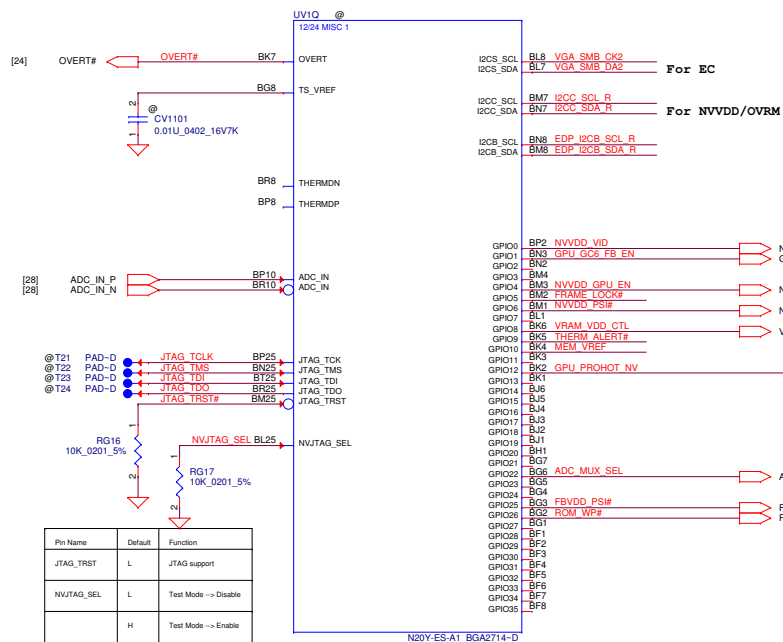
Under GPU

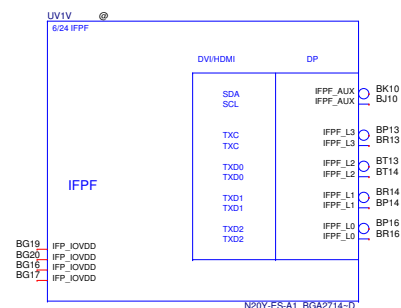
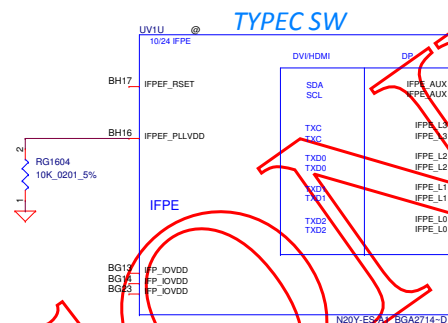
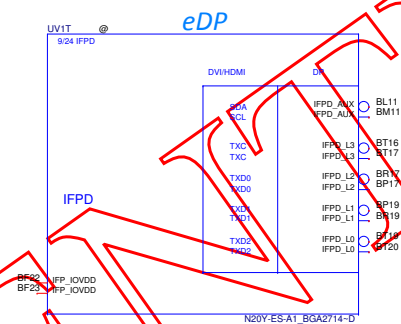
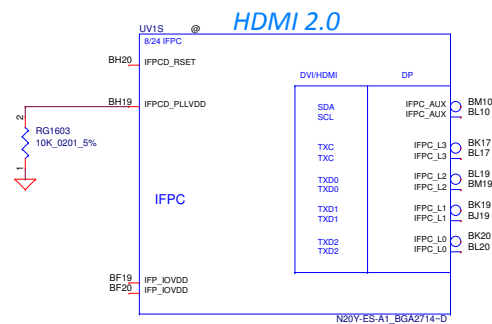
Near GPU

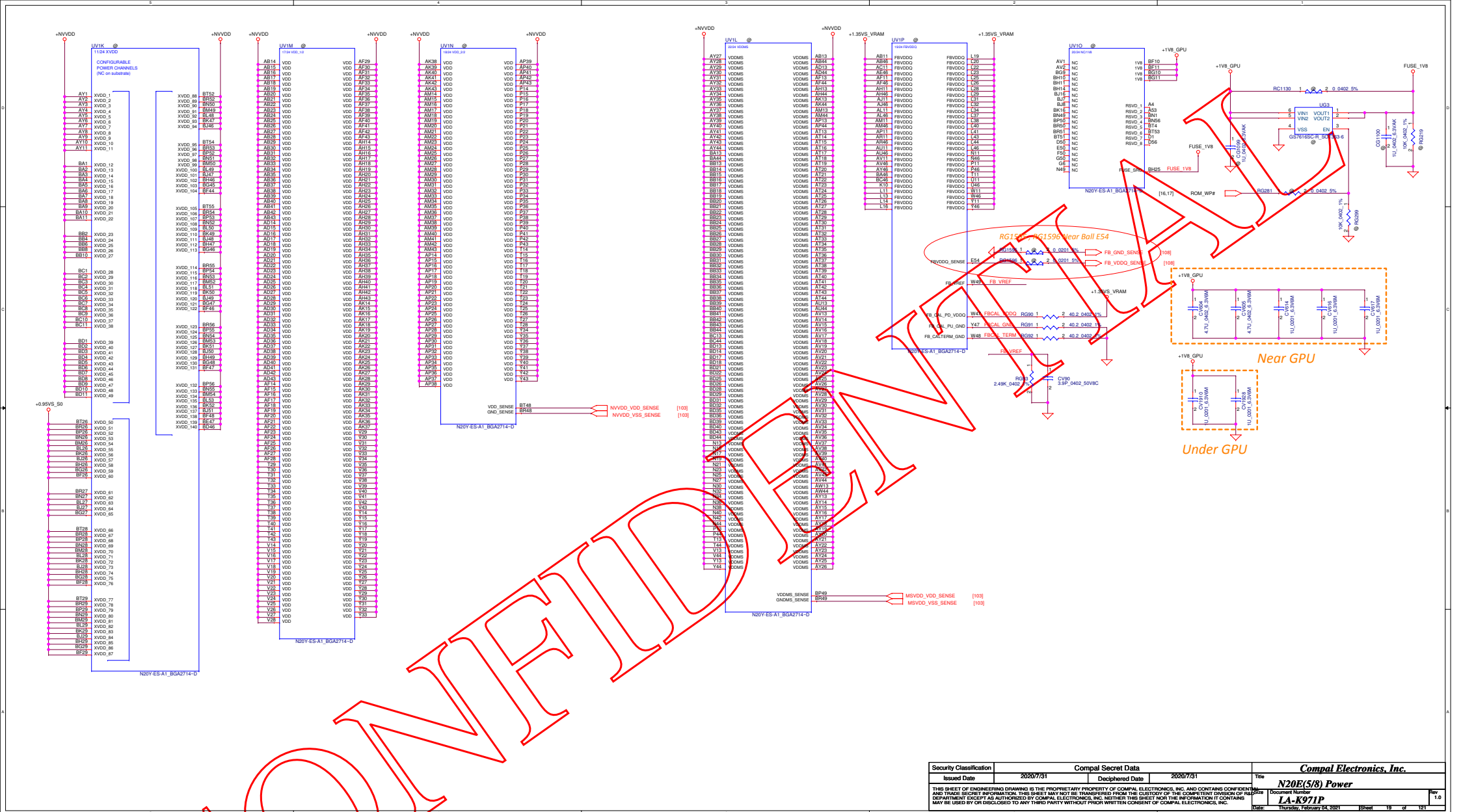
Near GPU

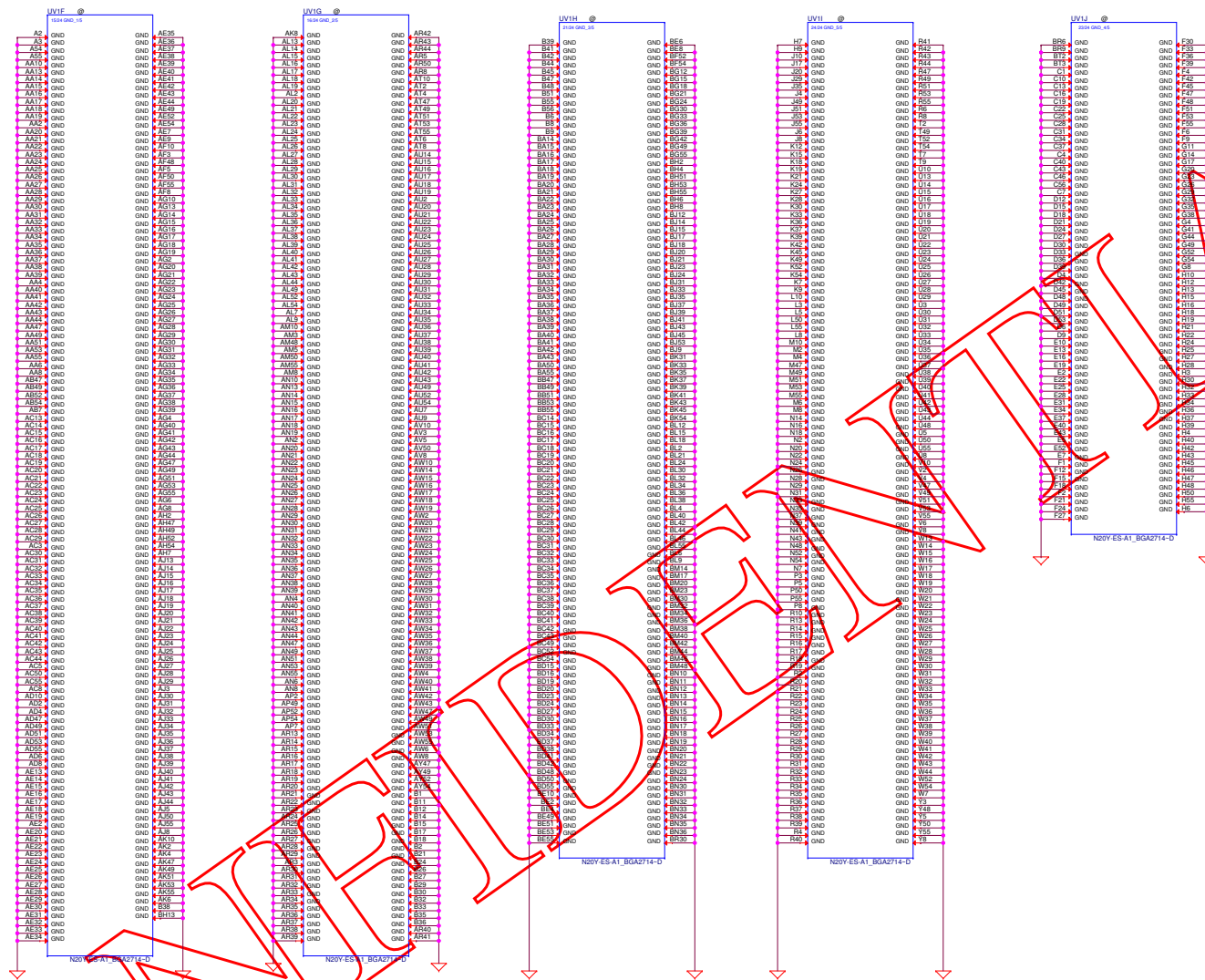
			Under GPU	Near GPU
IFP_IOVDD_x [x=1-15]	15	0.95V	5 x 4.7uF [0402 X6S]	3 x 4.7uF [0603 X6S]
PEX_DVDD_x [x=1-12]	12	0.95V	6 x 1uF [0402 X6S]	3 x 10uF [0805]
PEX_CVDD_x [x=1-3]			2 x 4.7uF [0603 X6S]	2 x 22uF [0805]
PEX_HVDD_x [x=1-13]	13	1.8V	9 x 1uF [0402 X6S]	3 x 10uF [0805]
PEX_PLL_HVDD			2 x 4.7uF [0603 X6S]	2 x 22uF [0805]
1V8_X [x=1-4]	4	1.8V	2 x 1uF [0402 X6S]	3 x 1uF [0402 X6S]
				2 x 4.7uF [0603 X6S]

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		LA-K97IP
		1.0

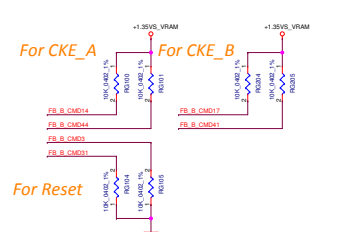
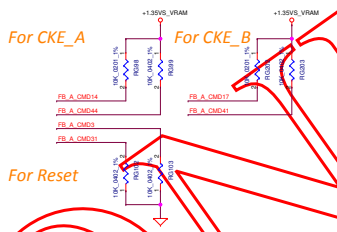
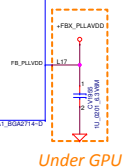
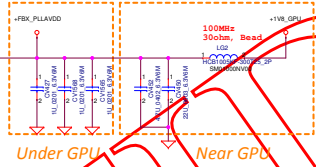
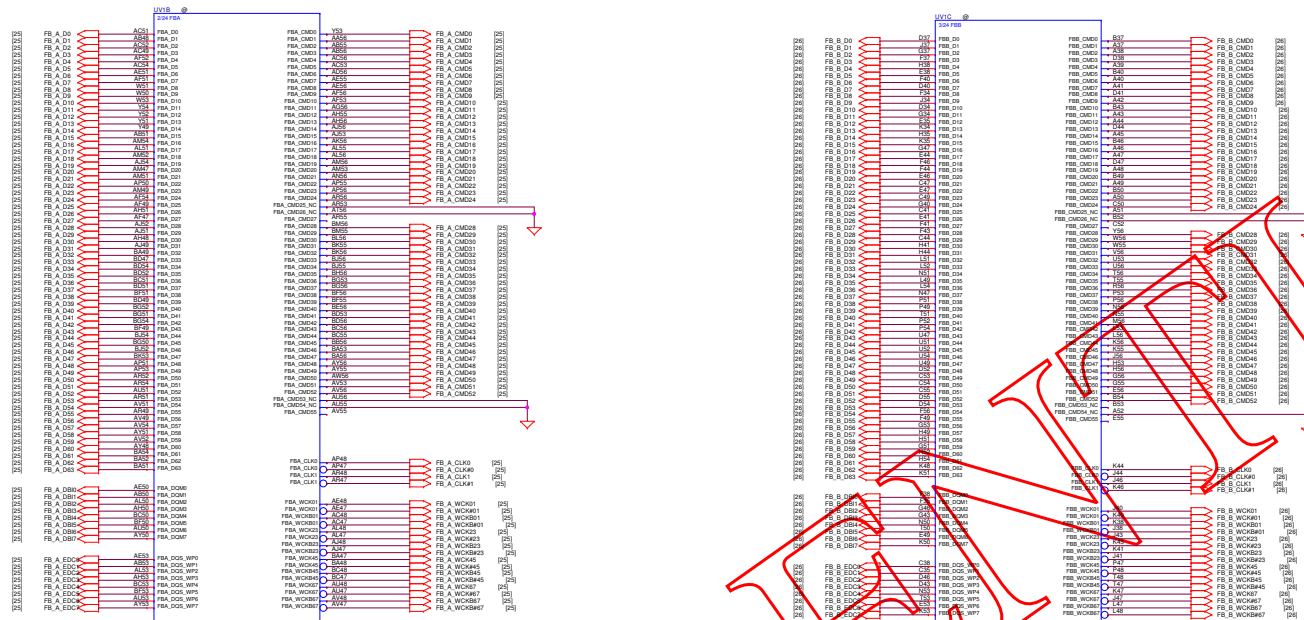




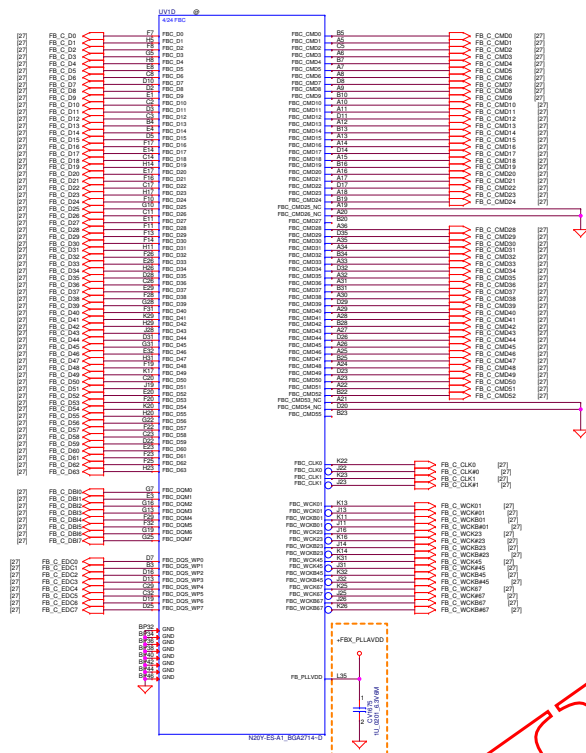




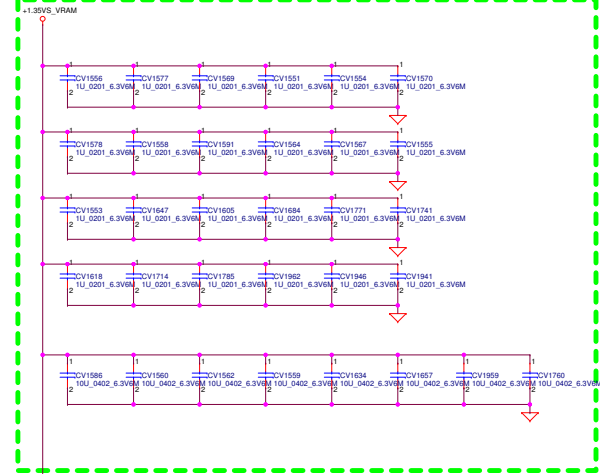
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				Date	Thursday, February 04, 2021 Sheet 20 of 121



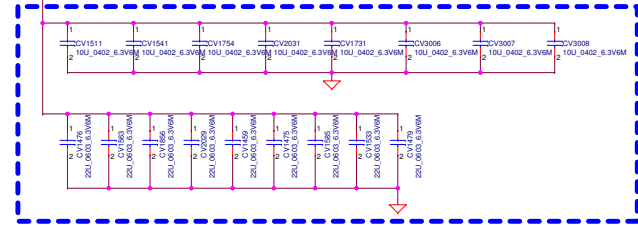
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FBVDDQ_GPU



Place under GPU
1uF_0402 X 24 pcs
10uF_0603 X 8 pcs



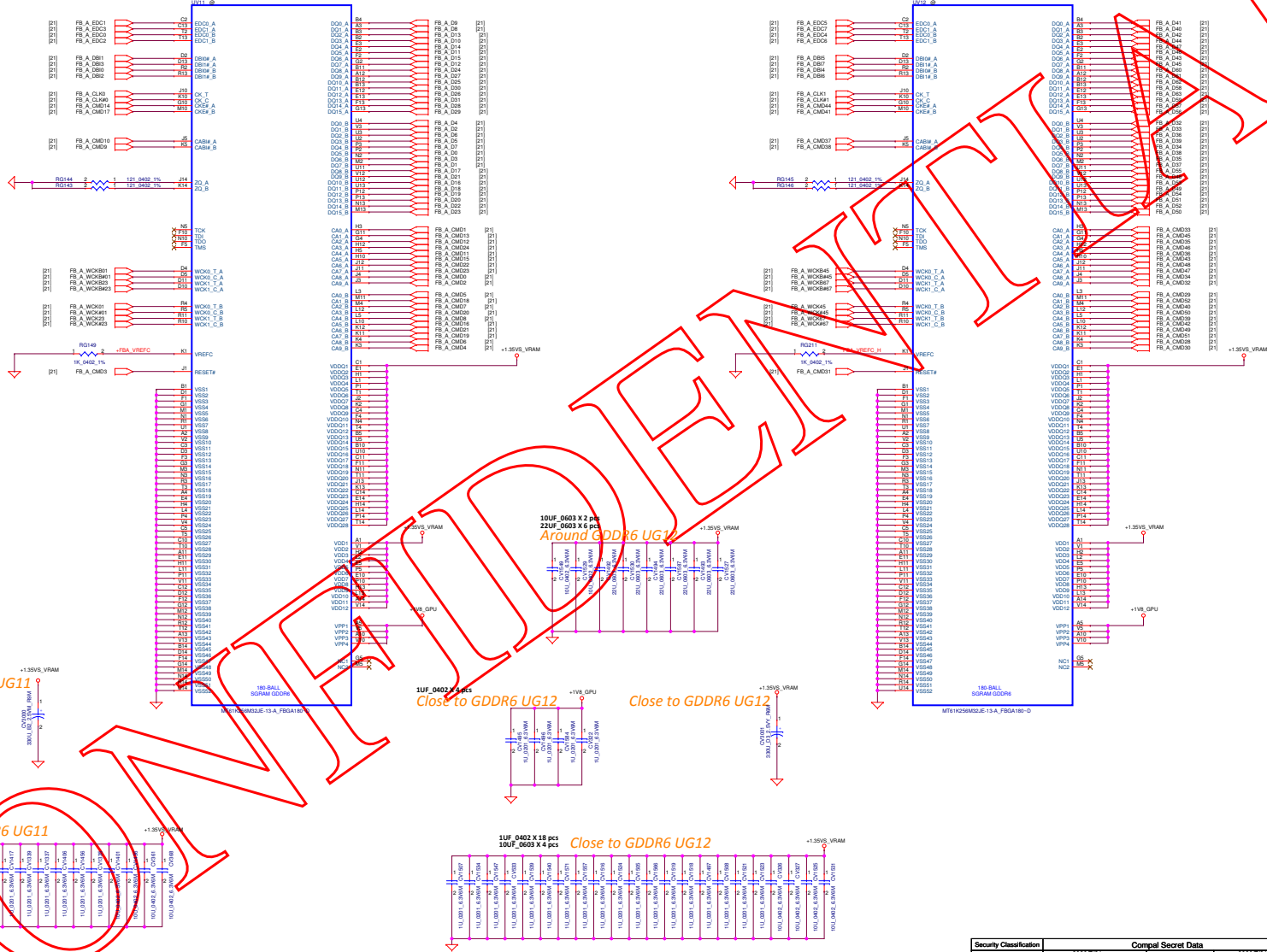
Place near GPU
22uF_0603 X 9 pcs
10uF_0603 X 5 pcs

Table 3.10 GB5-256 Power Rail Filtering

Rail [GPU Ball Name]	Balls	Voltage	Filtering under GPU	Filtering near GPU
NWDD	360	Varies	37 x 1uF [0402 X6S] 2 x 4.7uF [0603 X6S] 12 x 10uF [0603 X6S] 4 x 47uF [0805] Co-layout 3 x 330uF [7343 Poscap] OR [12 x 1uF [0402 X6S], 3 x 4.7uF [0603 X6S], 3 x 10uF [0603 X6S], 16 x 47uF [0805]]	Consult with Regulator vendor for regulator output bulk and decoupling capacitor recommendation.
MSVDD	248	Varies	29 x 1uF [0402 X6S] 11 x 10uF [0603 X6S] 3 x 47uF [0805] Co-layout: [1 x 330uF [7343 Poscap] OR [4 x 10uF [0603 X6S], 4 x 47uF [0805]]	Consult with Regulator vendor for regulator output bulk and decoupling capacitor recommendation.
FBVDDQ [GPU side]	58	1.20V 1.25V 1.35V	24 x 1uF [0402 X6S] 8 x 10uF [0603 X6S]	5 x 10uF [0603 X6S] 9 x 22uF [0603 X6S]

VRAM A

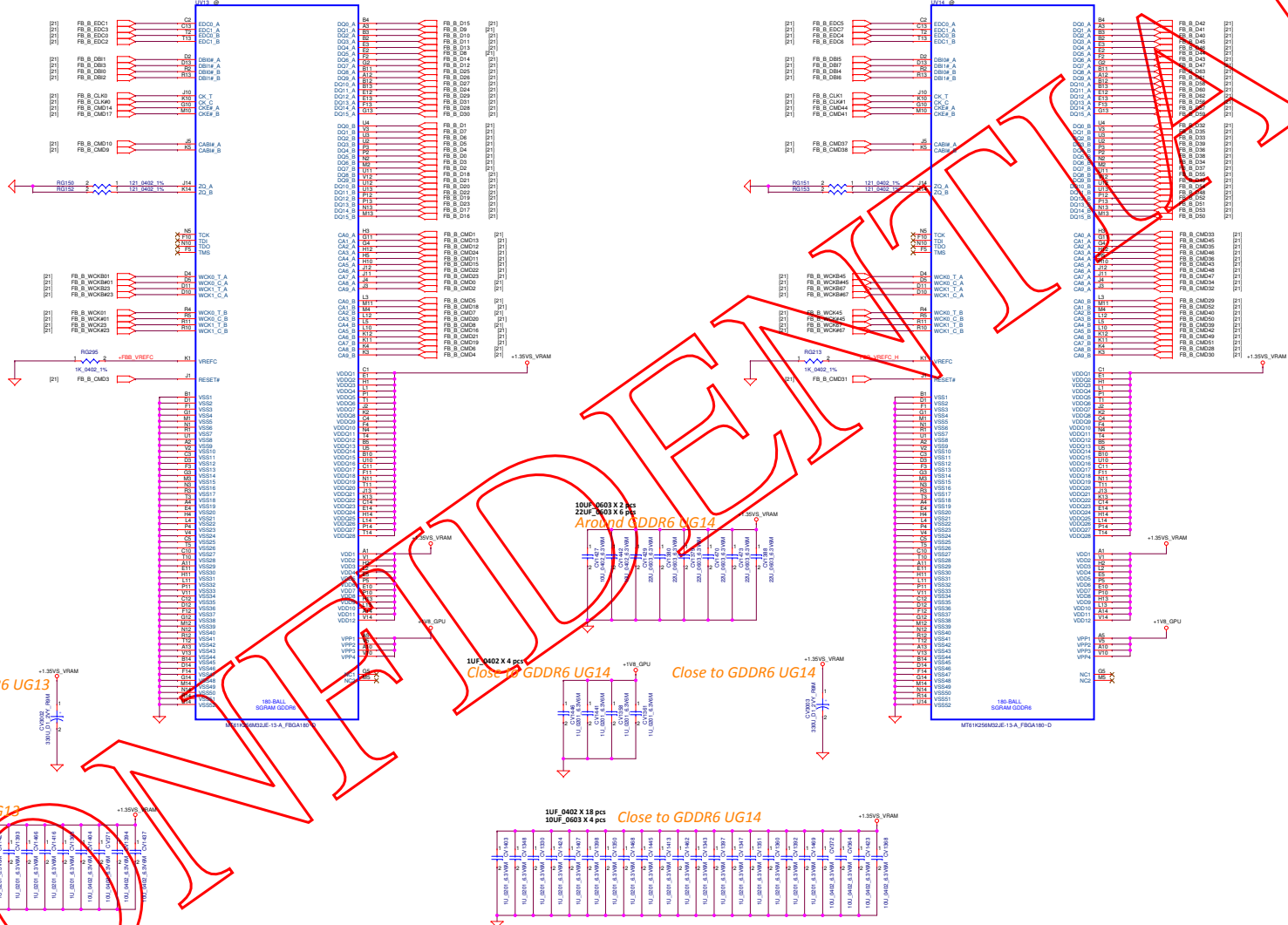
GDDR6 CMD Mapping		
Lower 0-31		Upper 32-63
DRAM1		DRAM2
Cmd-Byte 0-1		Cmd-Byte 4-5
CAD_A	CMD1	CMD33
CAL_A	CMD13	CMD45
CAL_A	CMD12	CMD35
CAL_A	CMD24	CMD46
CAL_A	CMD11	CMD36
CAL_A	CMD15	CMD43
CAL_A	CMD22	CMD48
CAL_A	CMD23	CMD47
CAL_A	CMD0	CMD34
CAL_A	CMD2	CMD32
CAL_A	CMD10	CMD37
CAL_A	CMD14	CMD44
CAL_B	CMD5	CMD29
CAL_B	CMD18	CMD52
CAL_B	CMD7	CMD40
CAL_B	CMD20	CMD50
CAL_B	CMD6	CMD39
CAL_B	CMD16	CMD42
CAL_B	CMD21	CMD49
CAL_B	CMD19	CMD51
CAL_B	CMD6	CMD28
CAL_B	CMD4	CMD30
CAL_B	CMD9	CMD38
CAL_B	CMD17	CMD41
RESET*	CMD3	CMD31



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				LA-K971P	
				Rev 1.0	

VRAM B

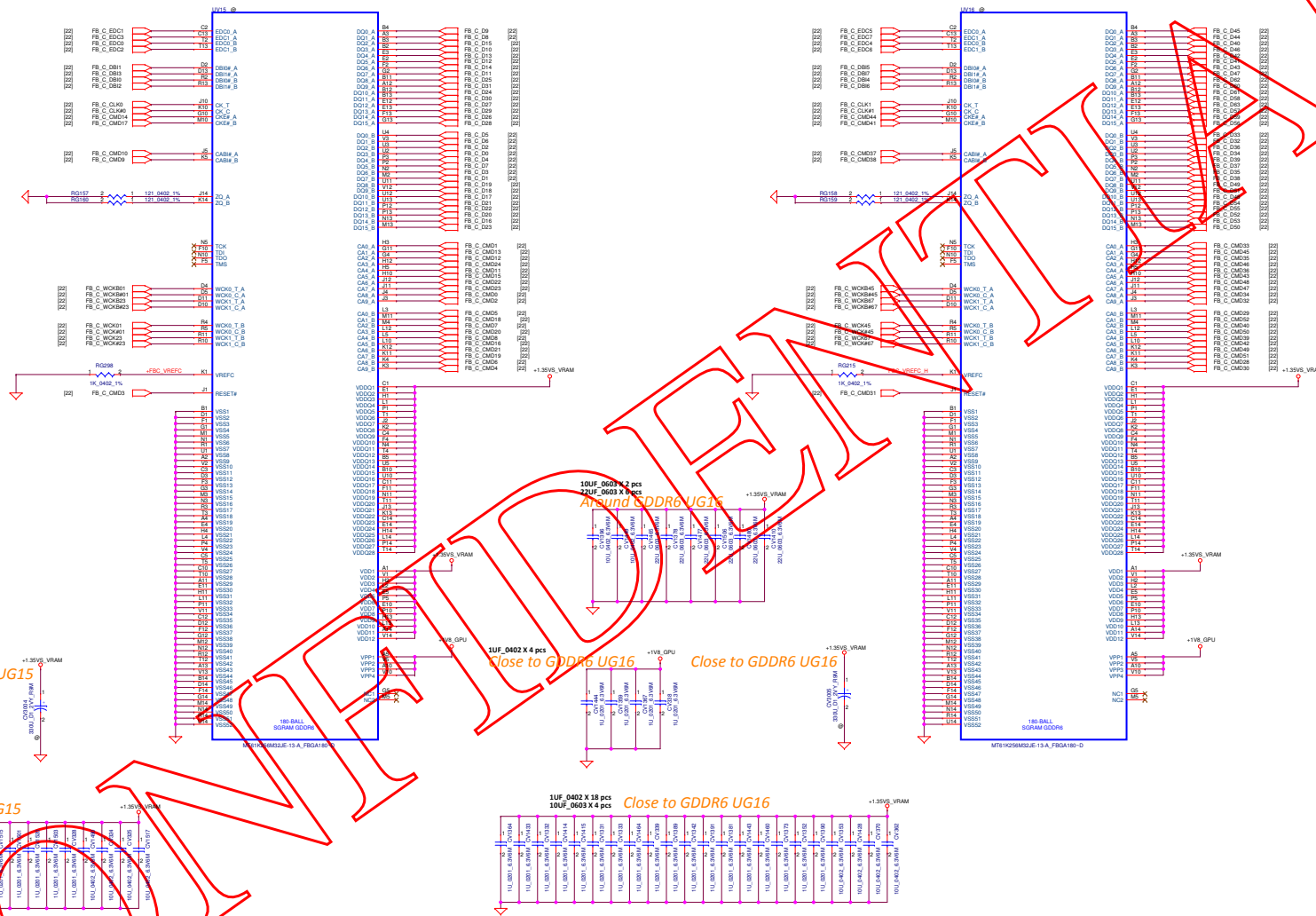
GA1XX GD06E CMD Mapping		
	Lower 0..31	Upper 32..63
	CH-Bit 0/1	DBMS2 CH-Bit 0/4,5
CAL_0	OMD1	OMD33
CAL_1	OMD13	OMD45
CAL_2	OMD12	OMD35
CAL_3	OMD14	OMD46
CAL_4	OMD11	OMD36
CAL_5	OMD15	OMD37
CAL_6	OMD3	OMD48
CAL_7	OMD3	OMD47
CAL_8	OMD2	OMD34
CAL_9	OMD3	OMD32
CAL_10	OMD3	OMD37
CAL_11	OMD3	OMD44
CH-Bit 0/1	2,4	CH-Bit 0/4,5
CAL_B	OMD5	OMD29
CAL_C	OMD18	OMD52
CAL_D	OMD17	OMD50
CAL_E	OMD30	OMD59
CAL_F	OMD19	OMD40
CAL_G	OMD16	OMD42
CAL_H	OMD6	OMD49
CAL_I	OMD19	OMD51
CAL_J	OMD6	OMD28
CAL_K	OMD4	OMD30
CAL_L	OMD19	OMD38
CAL_M	OMD17	OMD41
RESET*	OMD3	OMD31



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<p>DATE: 2020/7/31</p>			<p>Sheet 26 of 31</p>	

VRAM C (For E3)

GA1XX GDDR6 CMD Mapping		
Lower 0..31 CBA-Byte 0,1		Upper 32..63 CBA-Byte 4,5
CBA_0	CMD1	CMD33
CBA_1	CMD13	CMD43
CBA_2	CMD12	CMD35
CBA_3	CMD24	CMD46
CBA_4	CMD11	CMD36
CBA_5	CMD15	CMD43
CBA_6	CMD22	CMD48
CBA_7	CMD23	CMD47
CBA_8	CMD3	CMD34
CBA_9	CMD2	CMD37
CBA_10	CMD10	CMD32
CBA_11	CMD14	CMD44
CBA-Byte 2,3		CBA-Byte 6,7
CBA_0	CMD5	CMD29
CBA_1	CMD18	CMD52
CBA_2	CMD7	CMD40
CBA_3	CMD20	CMD39
CBA_4	CMD8	CMD30
CBA_5	CMD16	CMD42
CBA_6	CMD21	CMD49
CBA_7	CMD19	CMD51
CBA_8	CMD6	CMD38
CBA_9	CMD9	CMD41
CBA_10	CMD17	CMD45
CBA_11	CMD3	CMD31



Power Monitor(OVR-M)

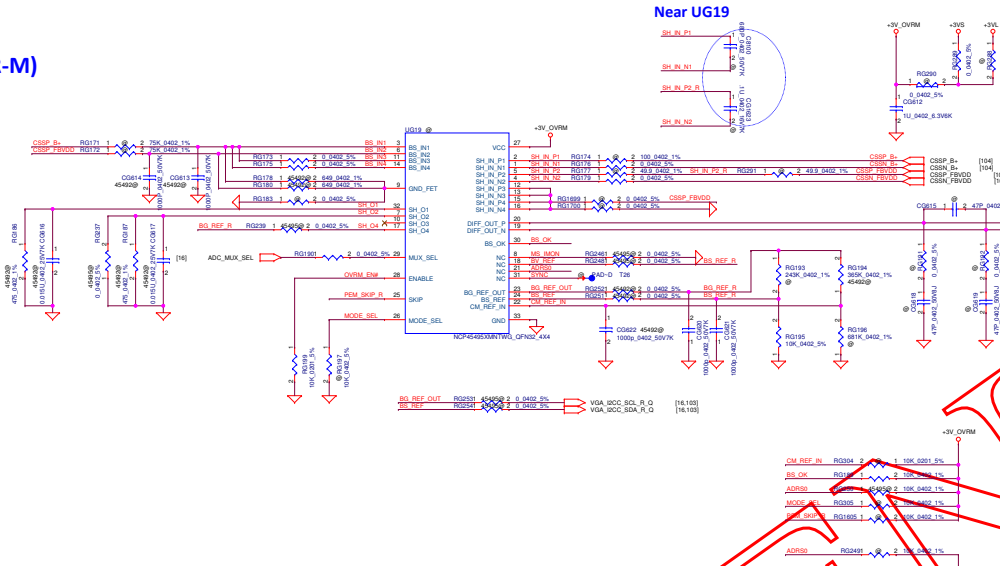
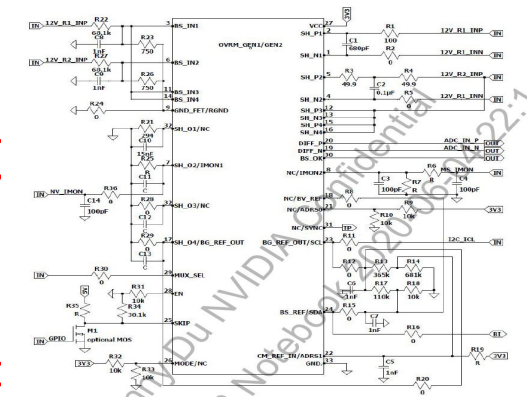


Figure 3.5 OVR-M GEN1 and GEN2 Co-Design



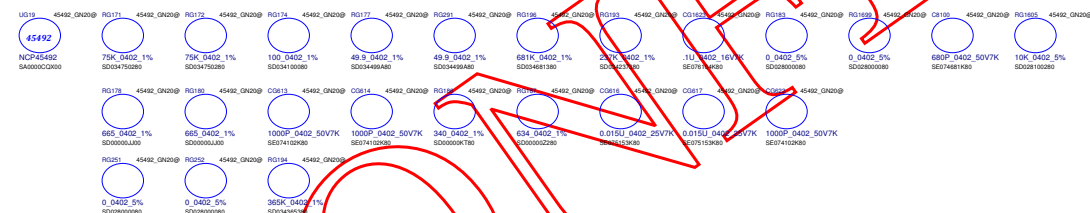
OVR-M Gen2



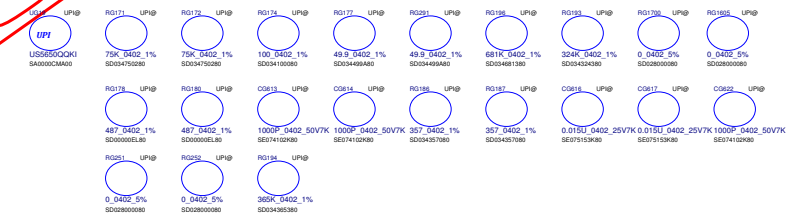
OVR-M Gen1 Onsemi (N18P-G61A)



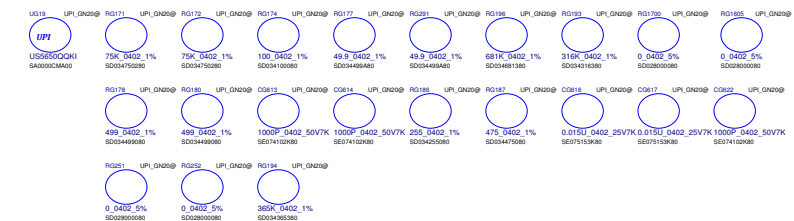
OVR-M Gen1 Onsemi (GN20)



~~OVR-M Gen1 UPI (N18P-G61A)~~



OVR-M Gen1 UPI (GN20)



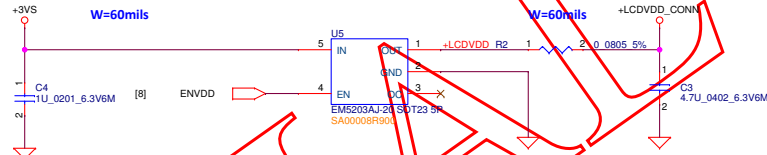
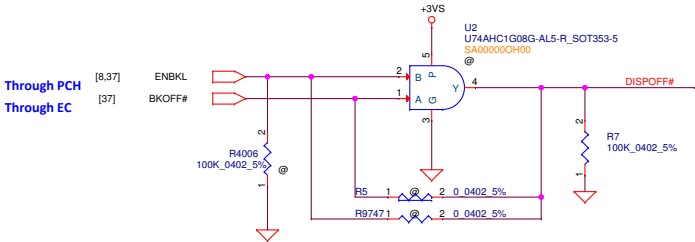
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CONFIDENTIAL

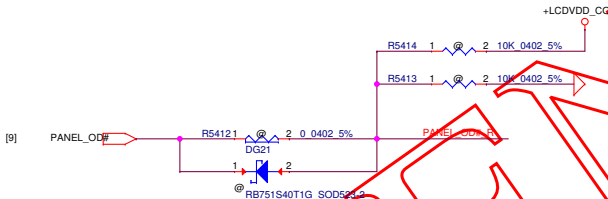
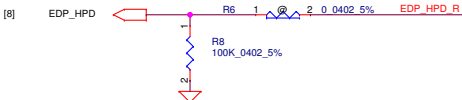
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DISPLAY OFF

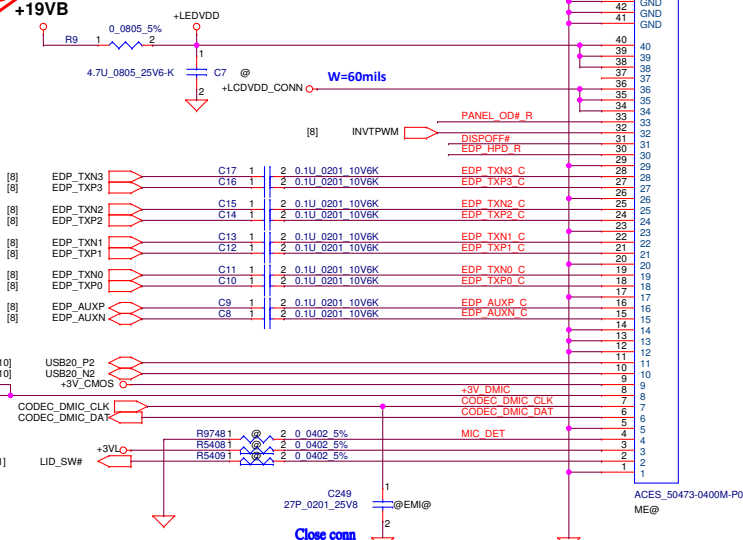
LCD POWER SWITCH



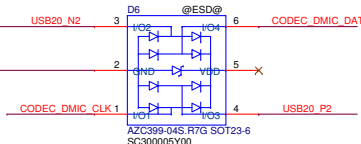
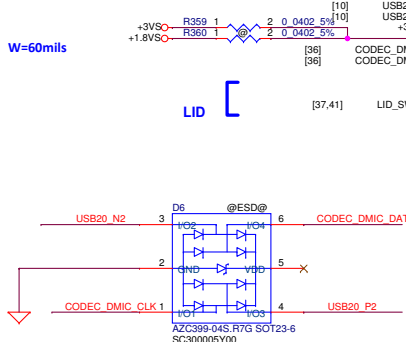
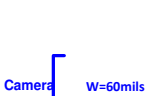
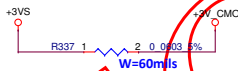
HOT PLUG DETECT

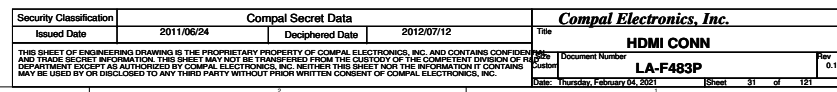


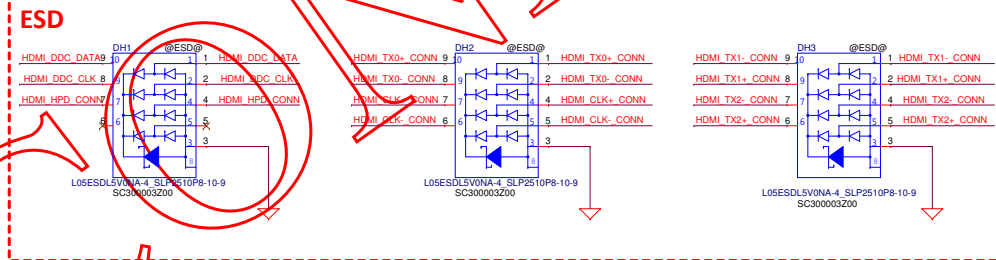
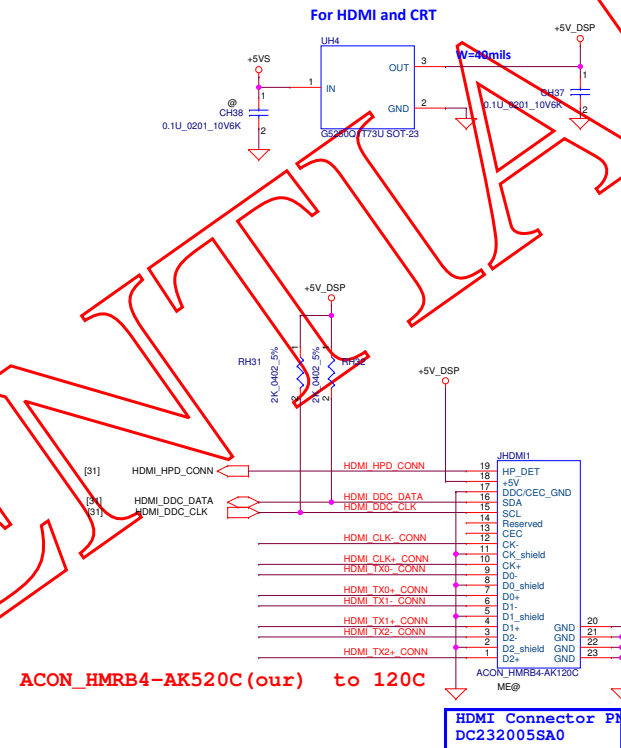
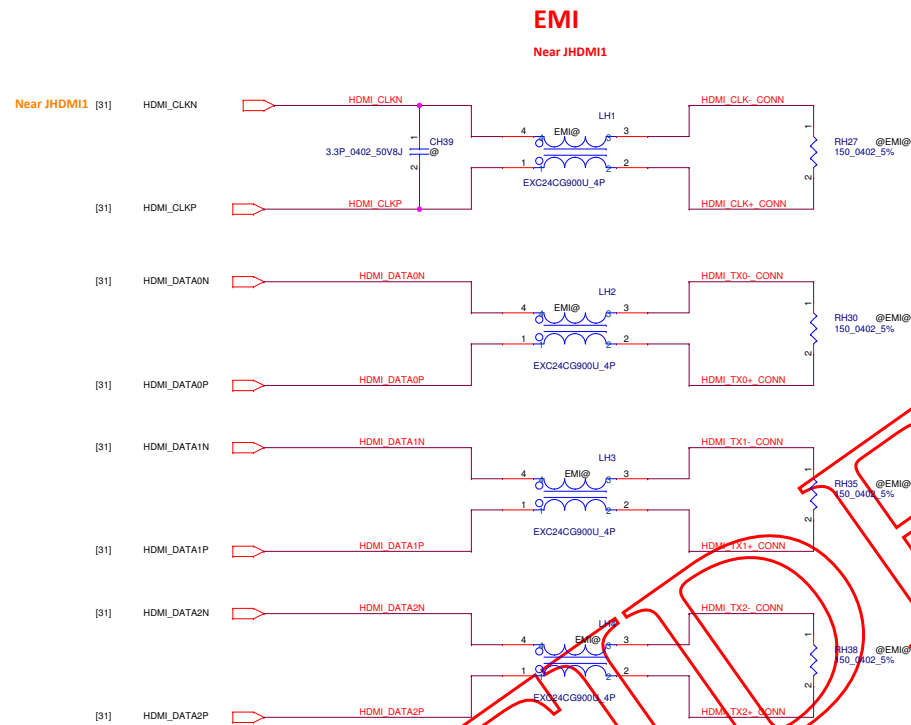
eDP CONNECTOR



CAMERA POWER CIRCUIT





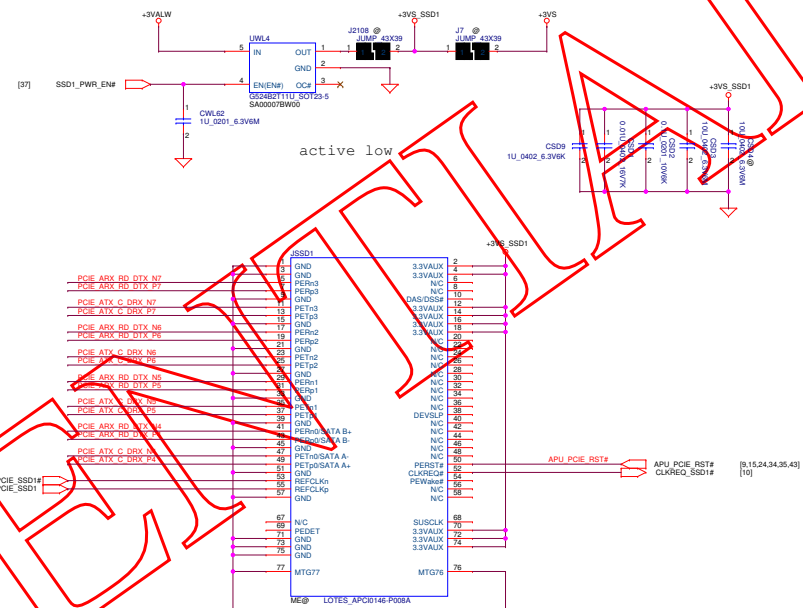
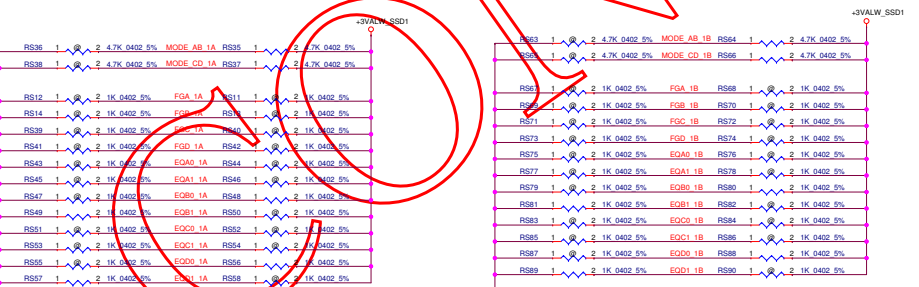
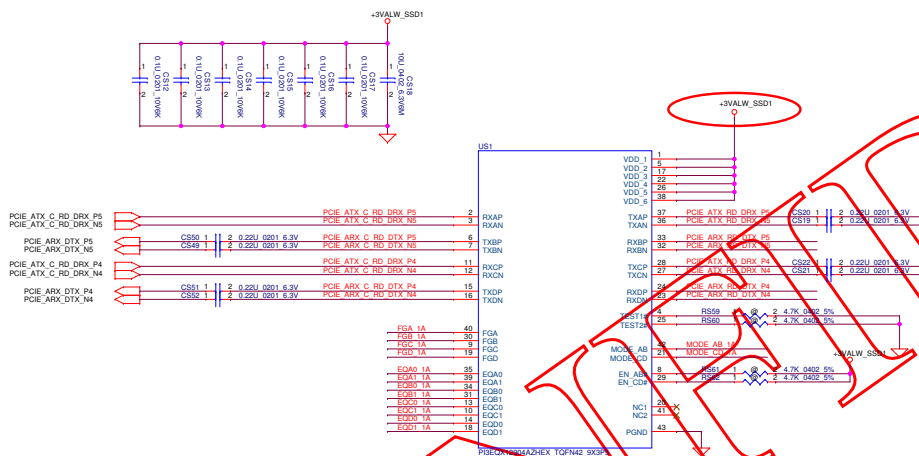
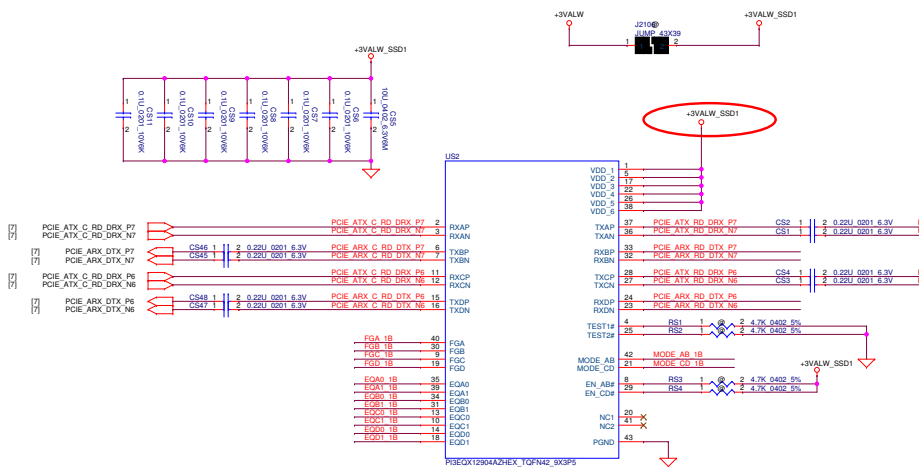


ACON_HMRB4-AK520C(our) to 120C

HDMI Connector Pin
DC232005SA0

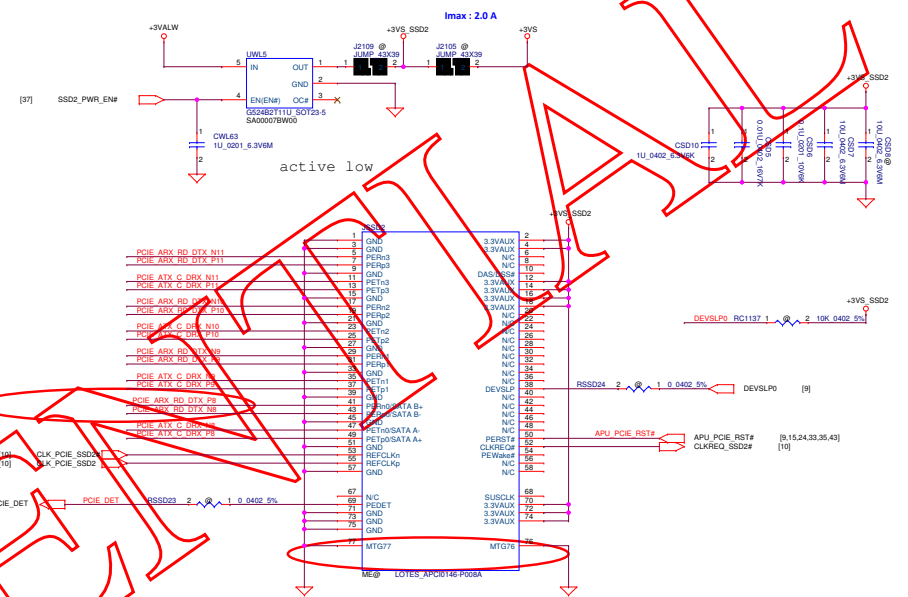
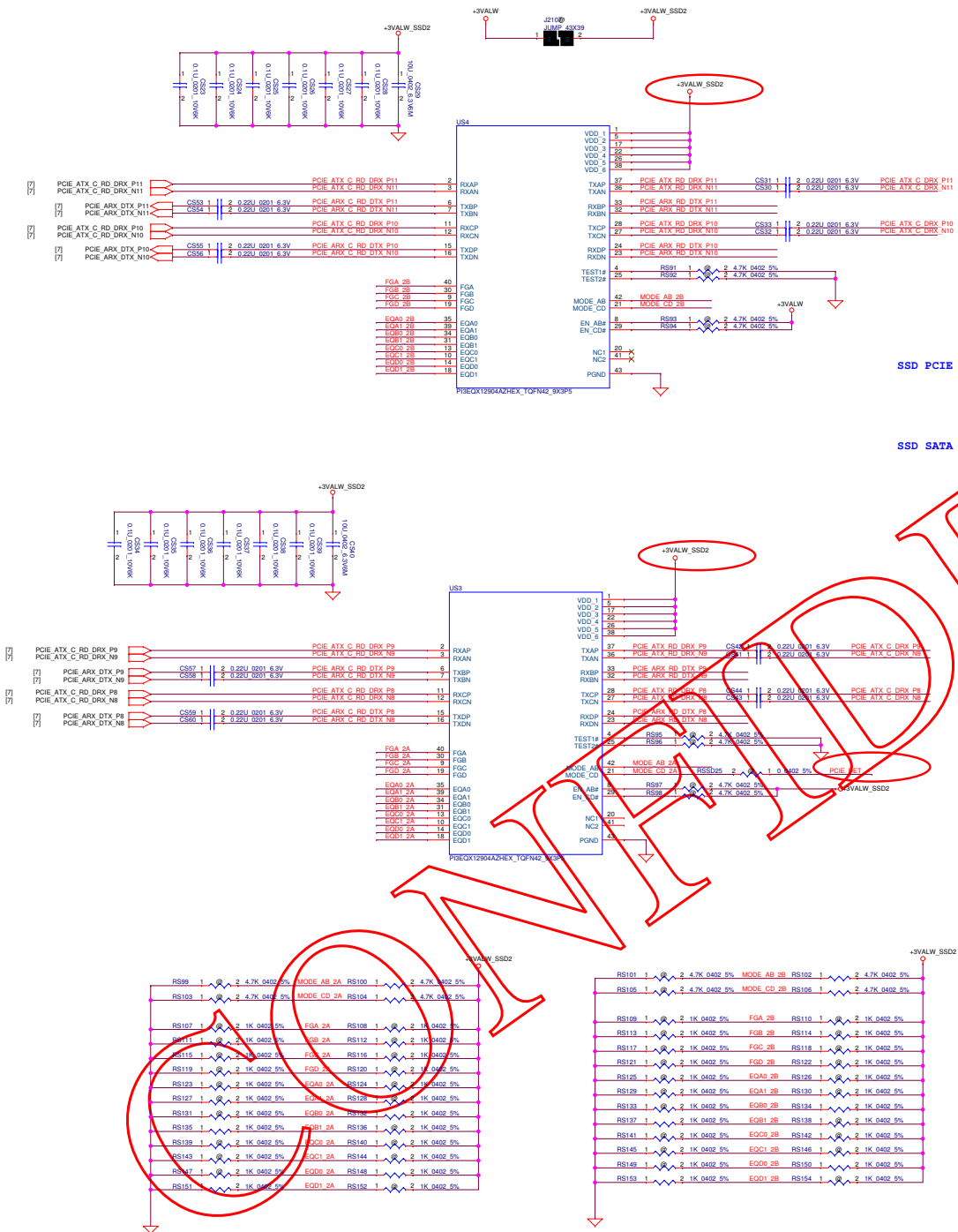
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SSD_2280 (TYPE M)



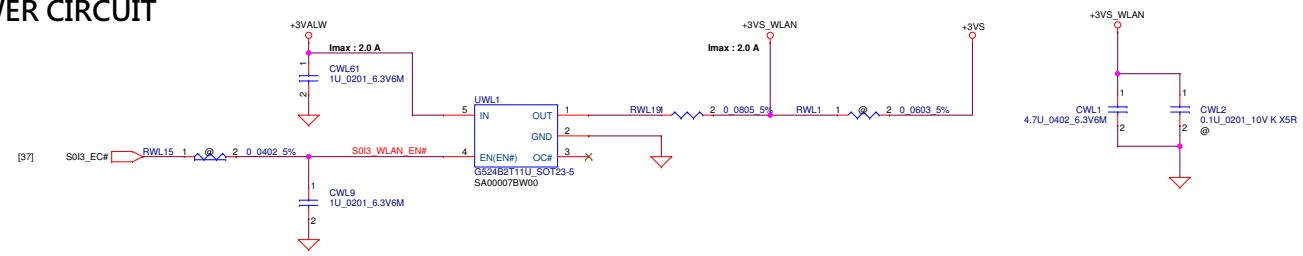
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SSD_2242 (TYPE M)

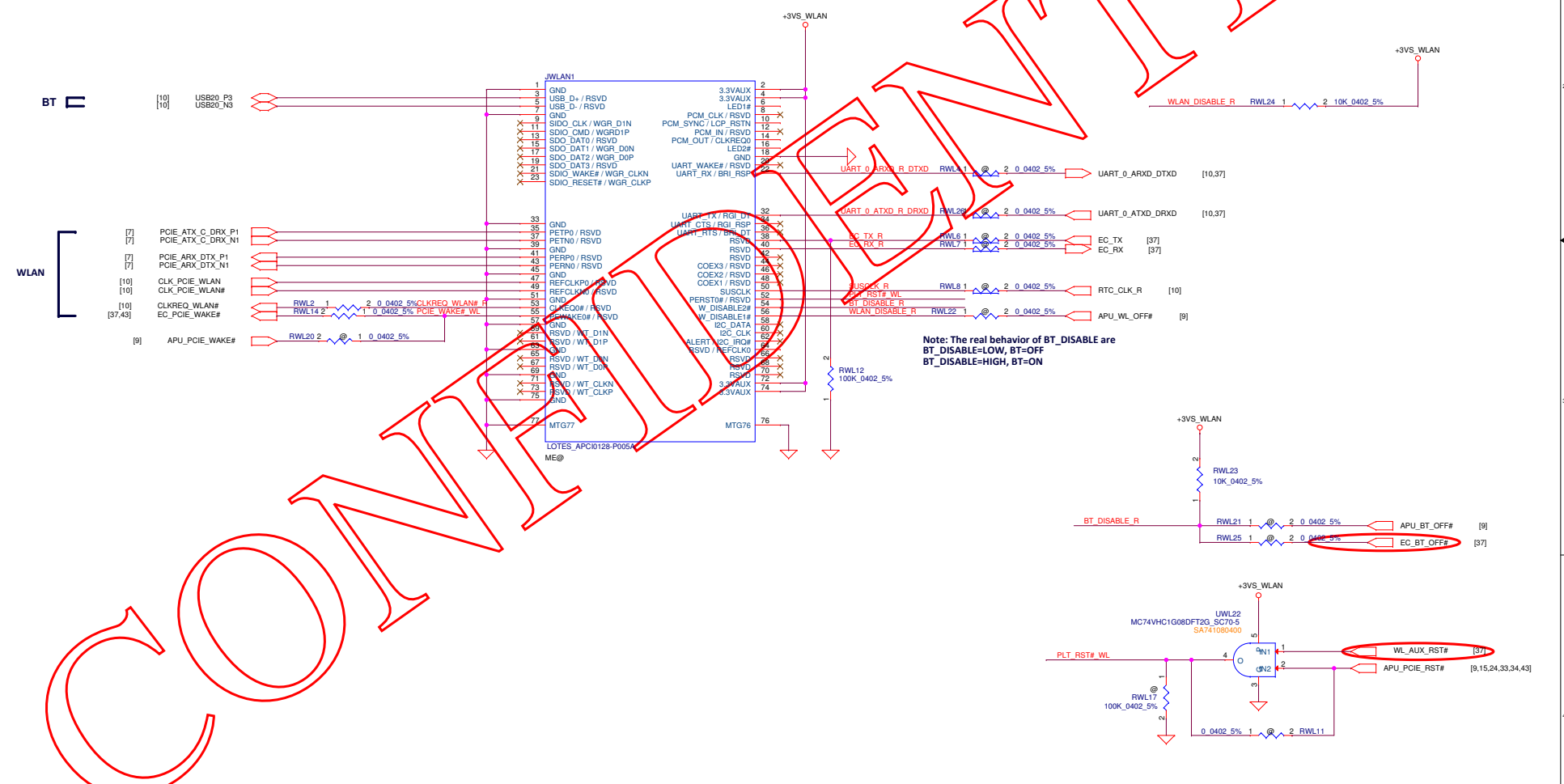


PEDET	Module Type
0	SATA
1	PCIE

WLAN POWER CIRCUIT

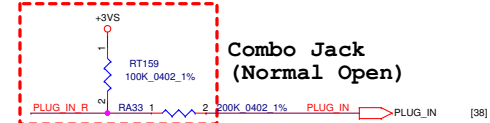
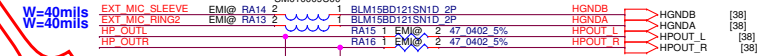
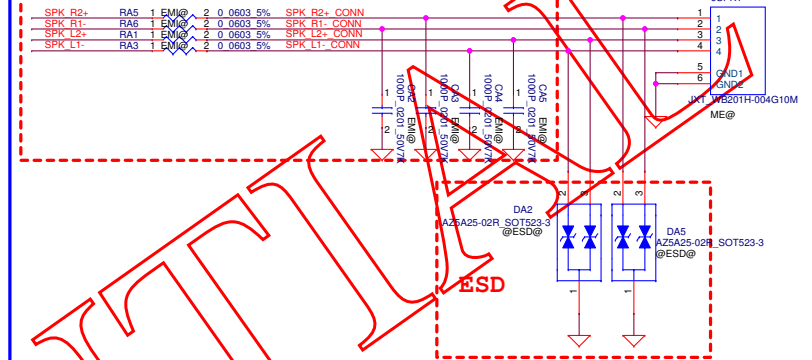
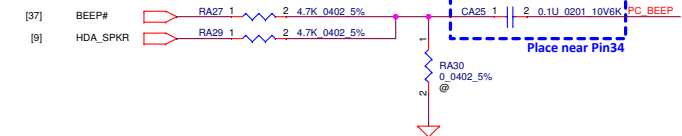


NGFF - WLAN / BT CONNECTOR (KEY-E)



Note: The real behavior of BT_DISABLE are
BT_DISABLE=LOW, BT=OFF
BT_DISABLE=HIGH, BT=ON

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			Document Number LA-J701P	
			Date: Thursday, February 04, 2021	Sheet 35 of 121

SPEAK 4 ohm : 40MIL
SPEAK 8 ohm : 20MILCombo Jack
(Normal Open)

+5VS --> +5VDDA_CODEC

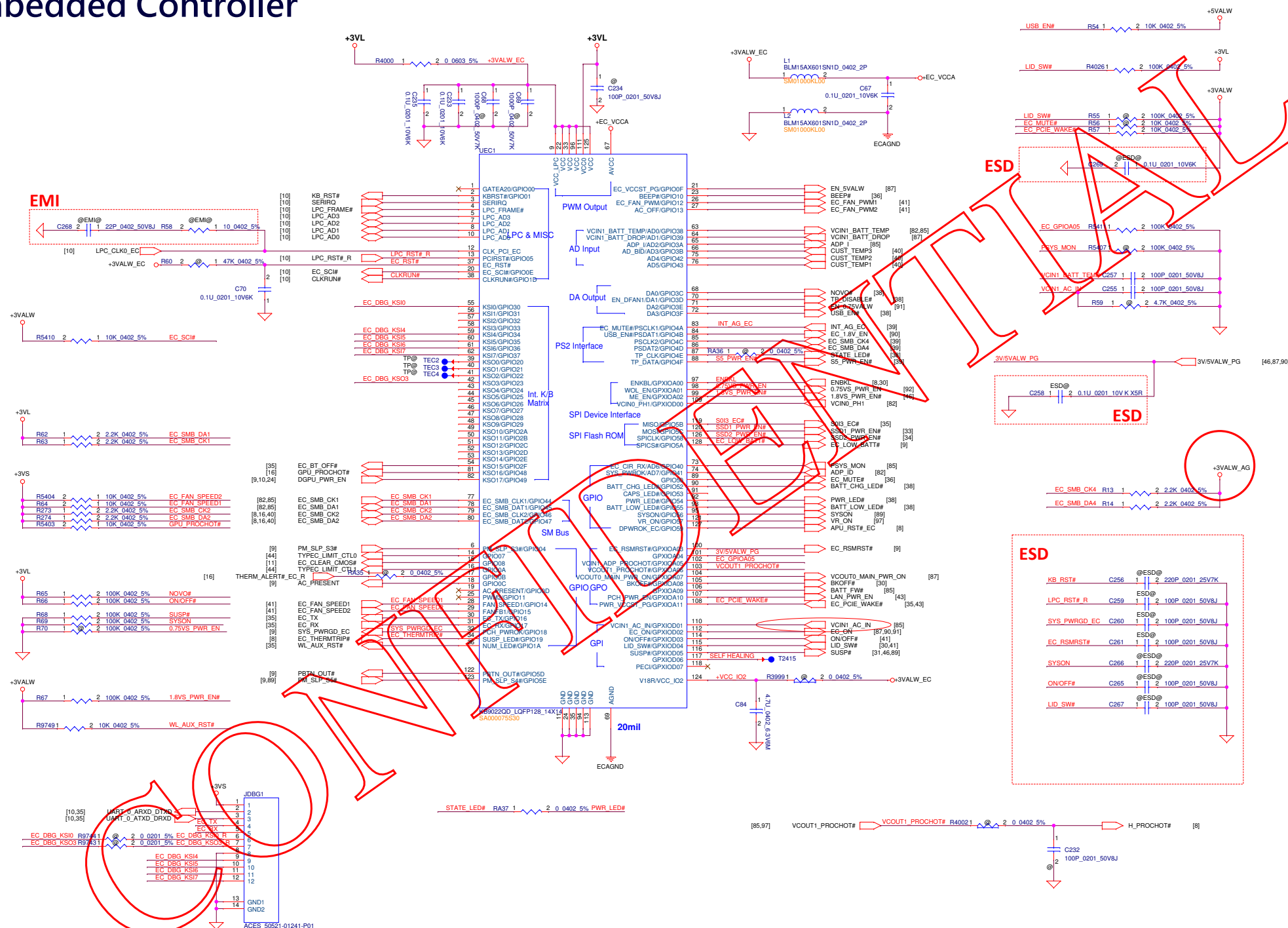
+1.8VS --> +1.8VDD_CODEC

+3VS --> +3VDD_CODEC

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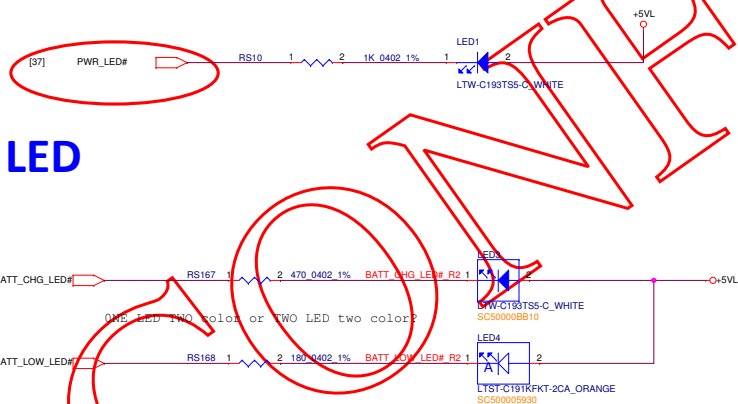
Security Classification	Compal Secret Data	Title	Compal Electronics, Inc.
Issued Date	2019/08/07	Deciphered Date	2020/12/31
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Document Number		Audio ALC256&711/Audio Conn.	
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Embedded Controller

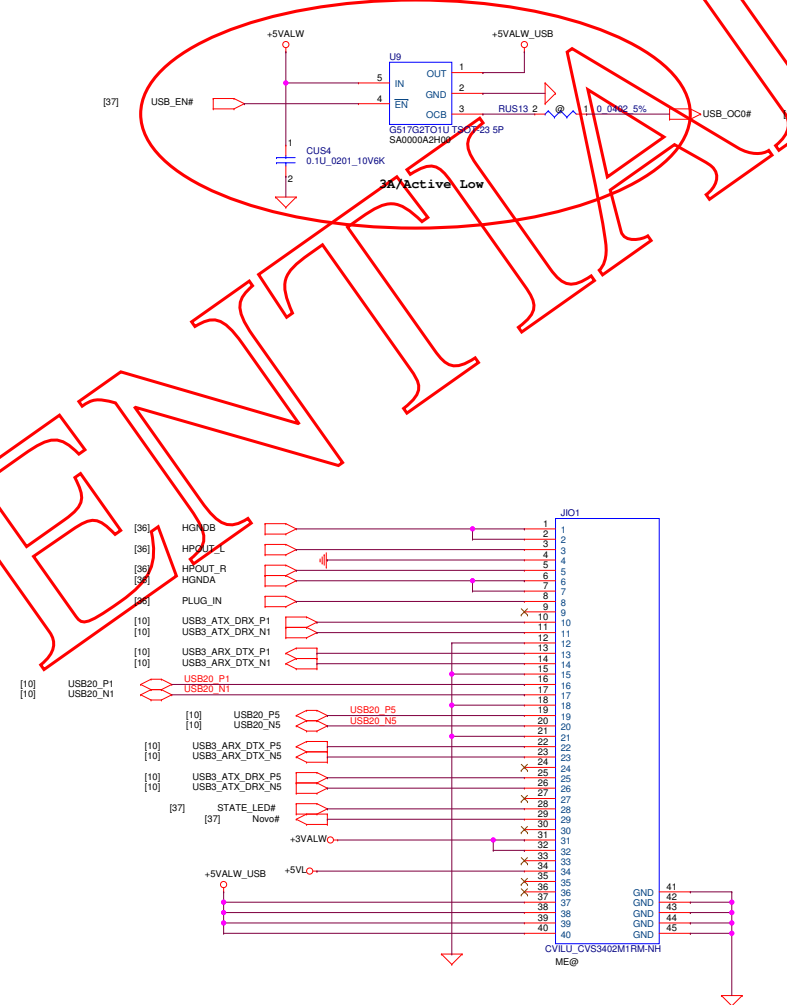


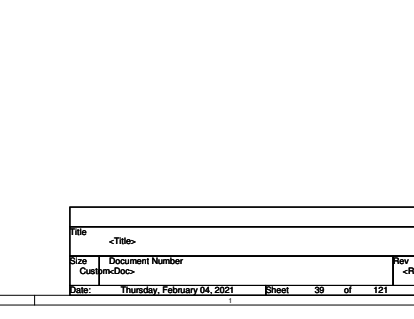
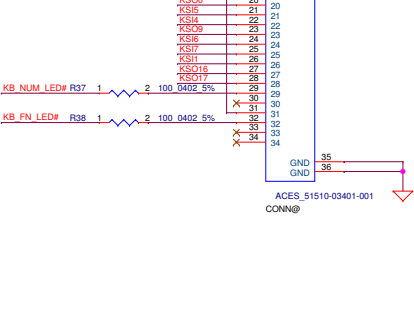
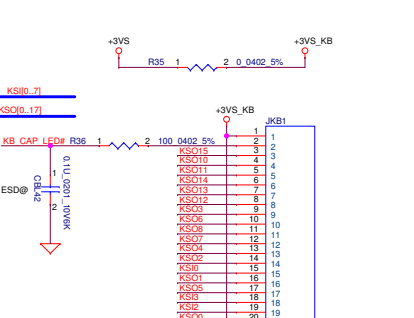
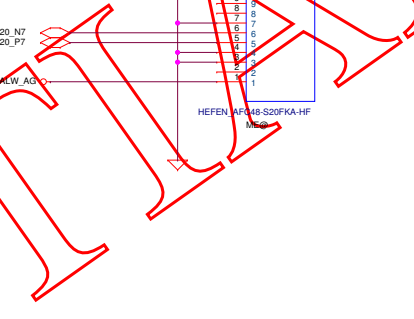
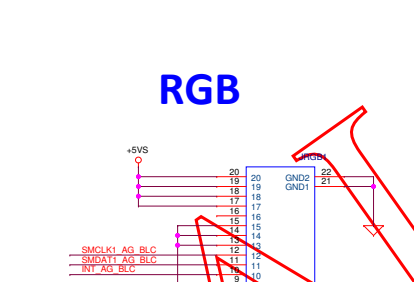
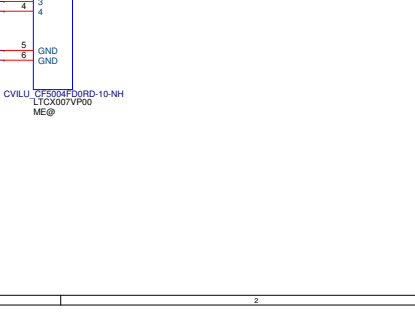
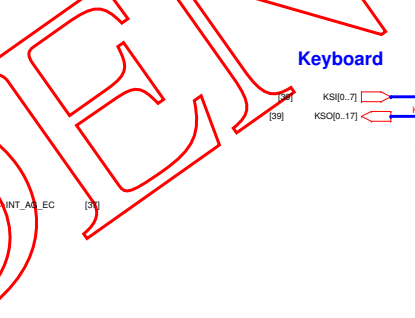
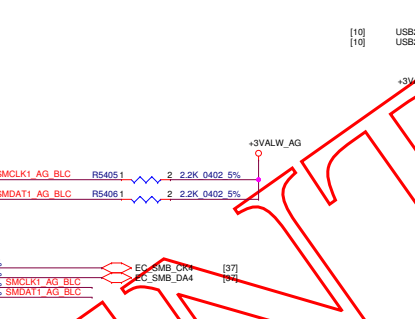
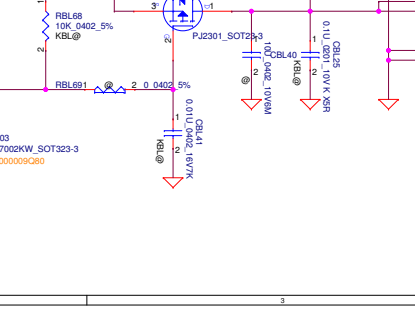
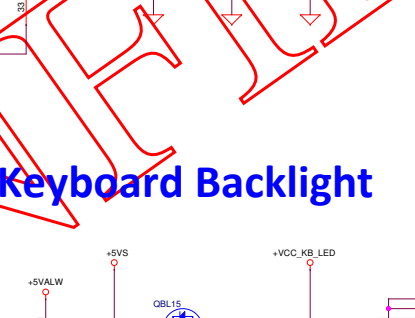
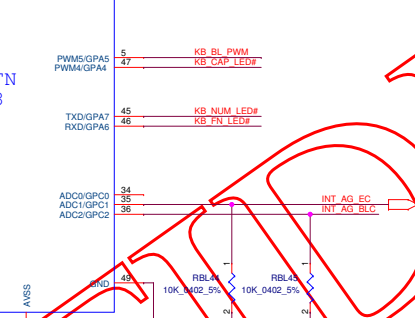
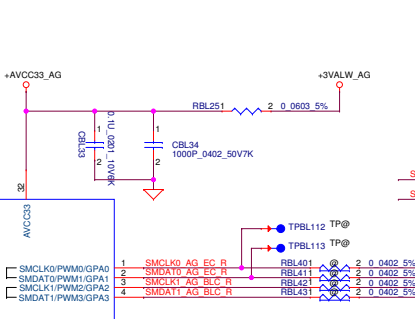
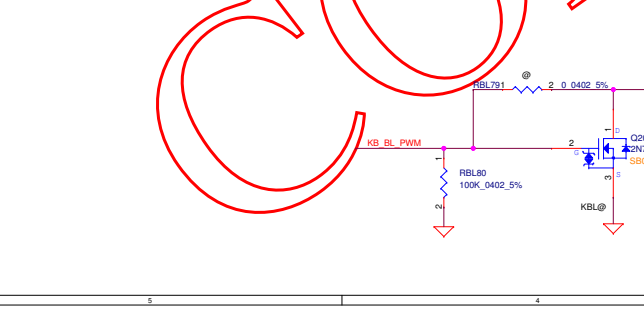
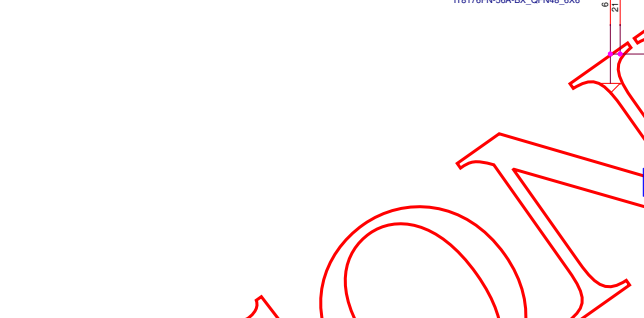
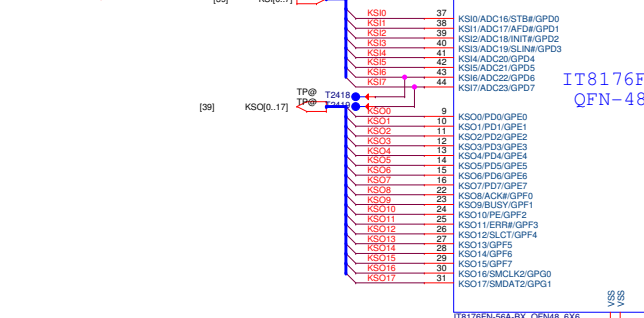
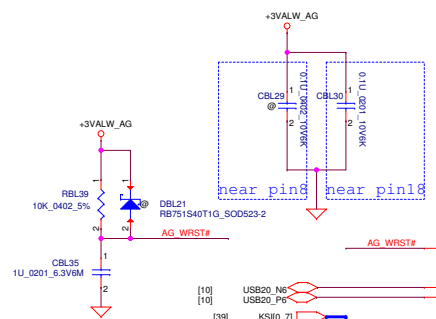
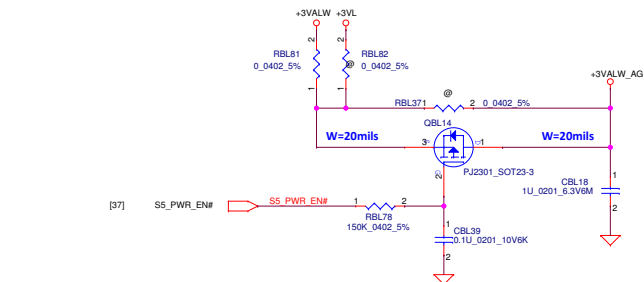
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Issued Date	2020/7/31	Deciphered Date	2020/7/31	Title	EC KB9542Q
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BATT LED



change from SA00007BW00 to SA0000A2H00





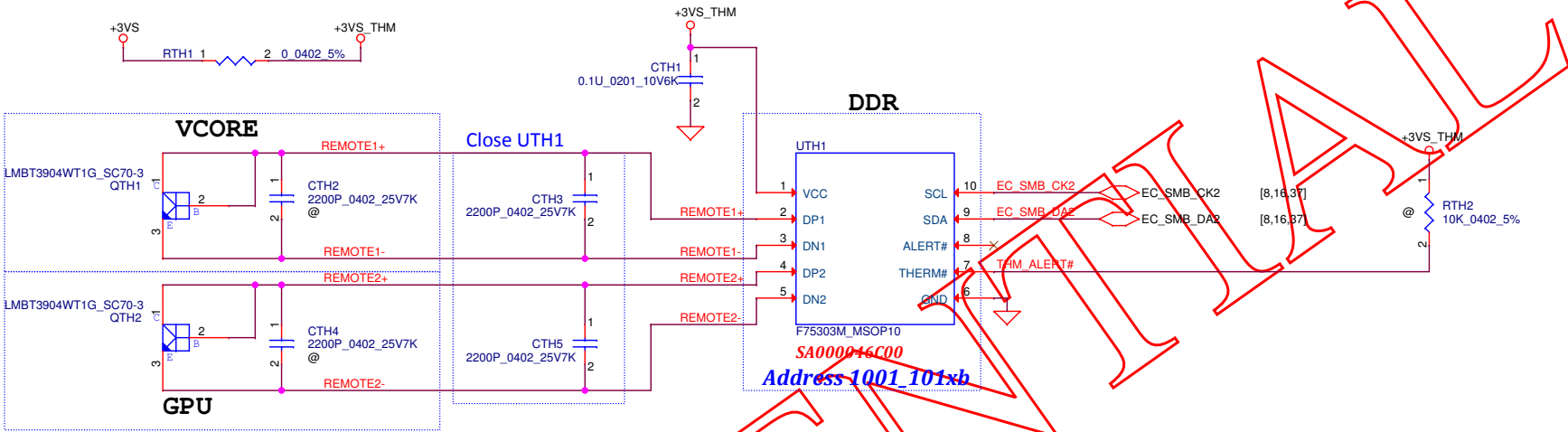
RGB

Keyboard

Keyboard Backlight

File	<Title>	Rev
Size	Document Number	CustomDoc
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THERMAL SENSOR For Smart Performance

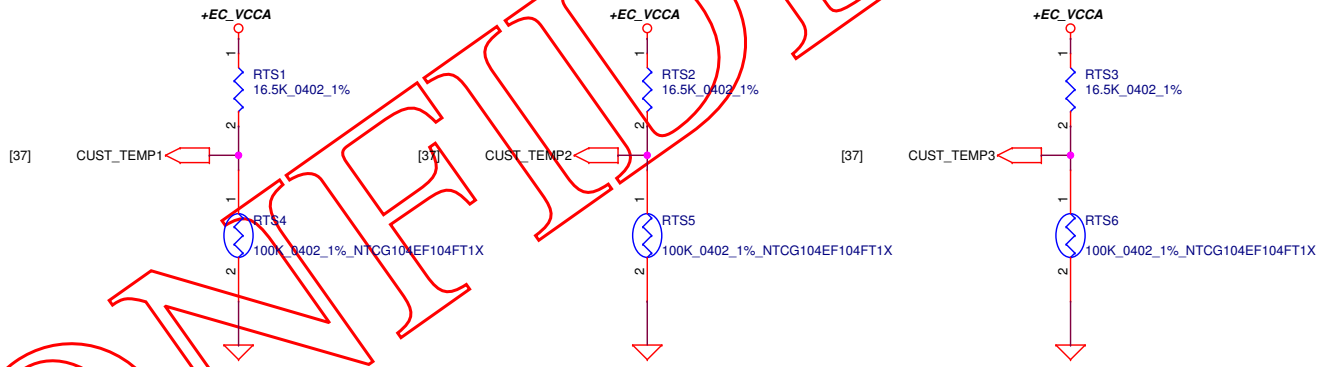


REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"

CPU Fan

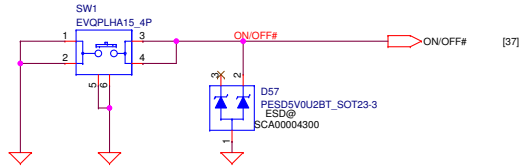
GPU Fan

SSD



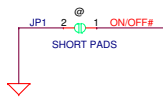
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Issued Date	2020/7/31	Deciphered Date	2020/7/31	Title	Thermal Sensor
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Power Button

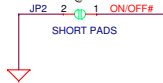


ON/OFF# SHORT PAD

TOP side



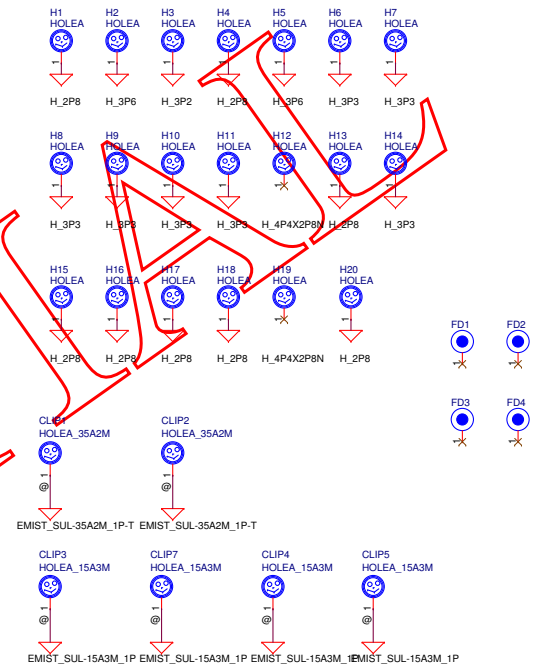
BOTT side



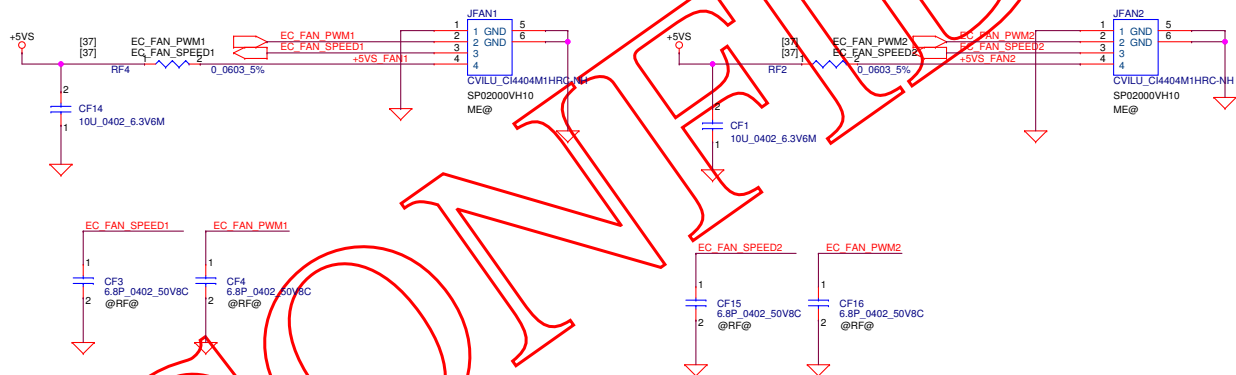
LID

SCREW

CLIP



FAN



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Issued Date	2020/04/09	Deciphered Date	2022/04/09	Rev
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Compal Electronics, Inc.

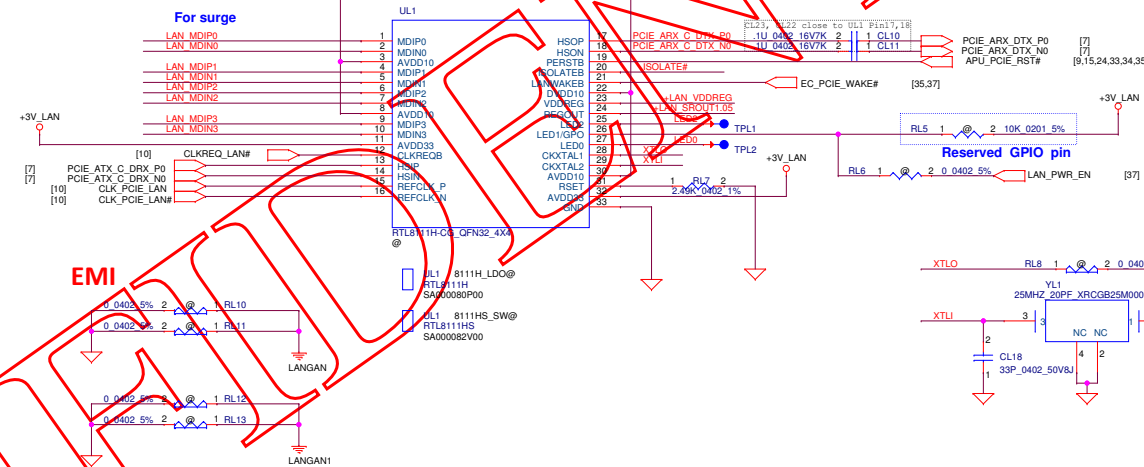
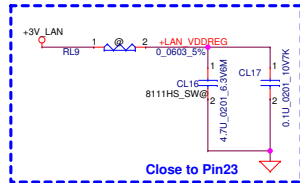
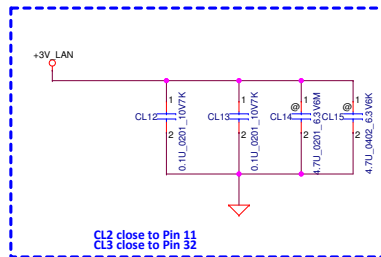
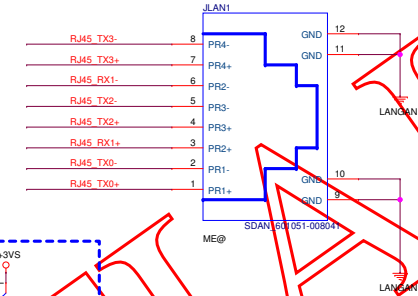
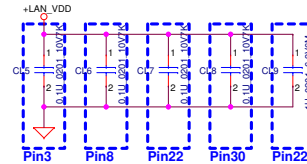
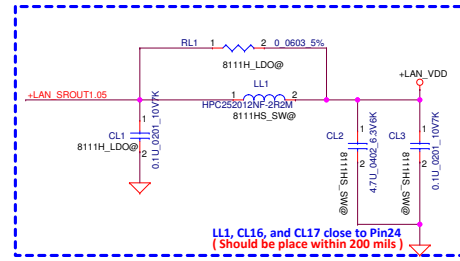
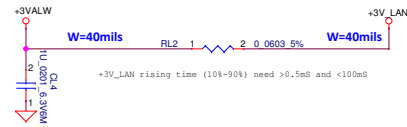
PCB PN / SCREW / FAN

LA-J701P

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Issued Date	2016/12/05	Deciphered Date	2017/04/03	Title	M.2 SSD/HDD	
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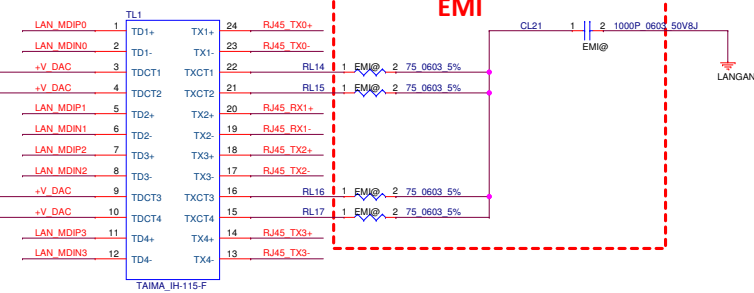
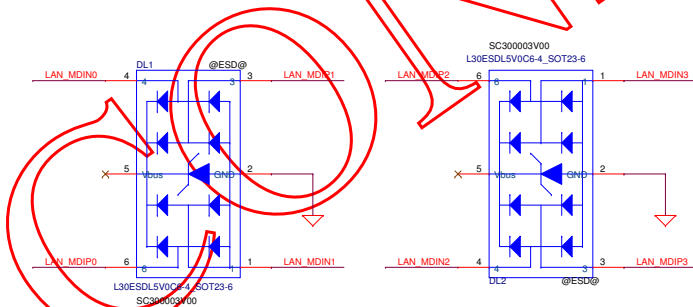
RJ-45 CONN.



EMI

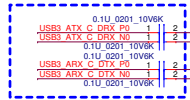
EMI

EMI

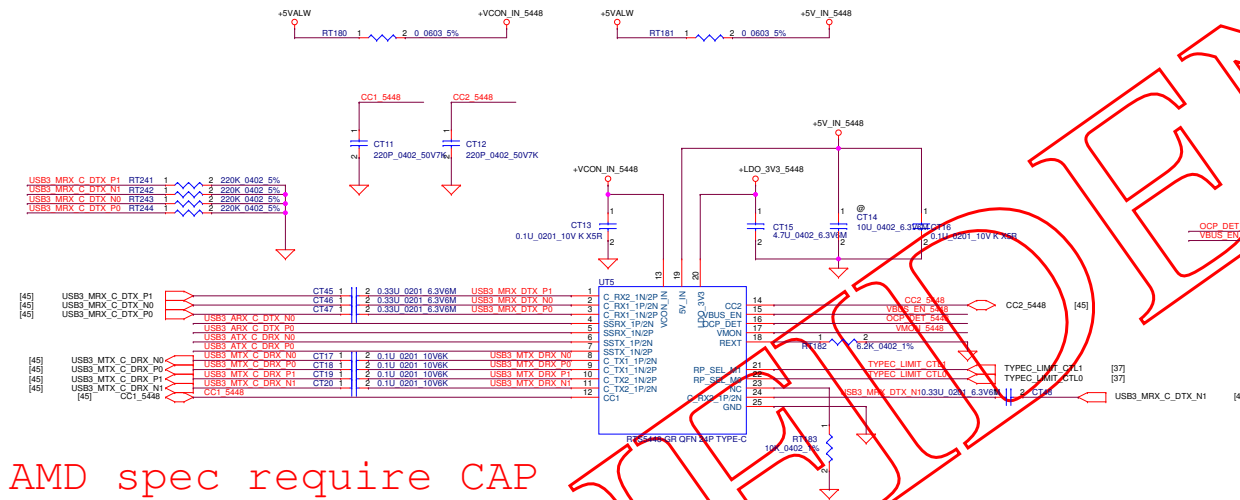
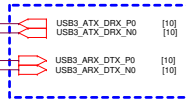


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Issued Date	2020/7/31	LAN_RTL8111H/RTL8107E
Deciphered Date	2020/7/31	Document Number
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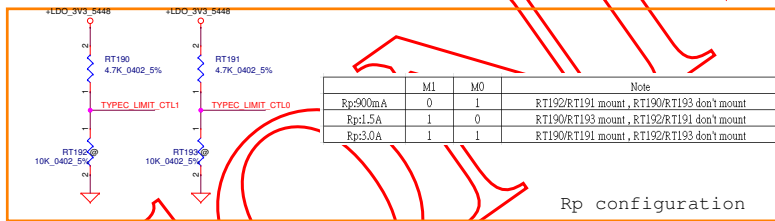
TO Connector



From APU

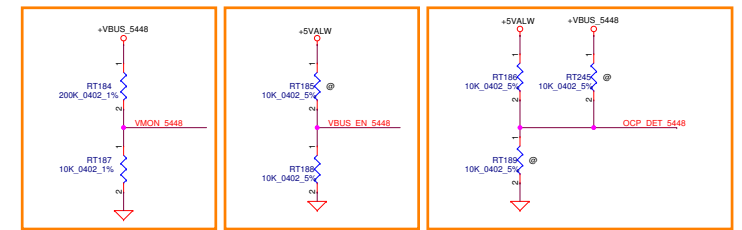
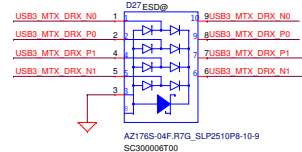
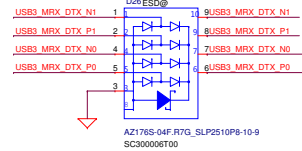


AMD spec require CAP



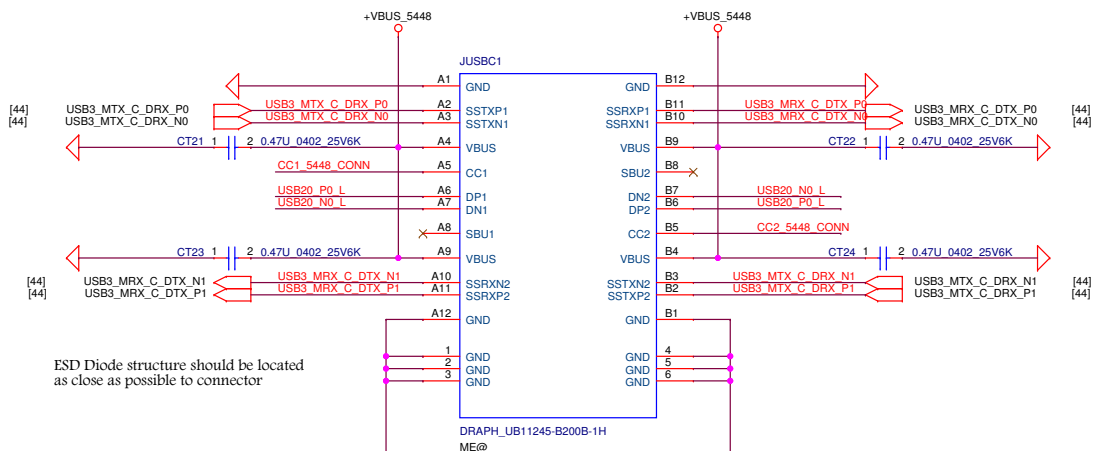
	M1	M0	Note
Rp=900mA	0	1	RT192/RT191 mount, RT190/RT193 don't mount
Rp=1.5A	1	0	RT190/RT193 mount, RT192/RT191 don't mount
Rp=3.0A	1	1	RT190/RT191 mount, RT192/RT193 don't mount

Rp configuration



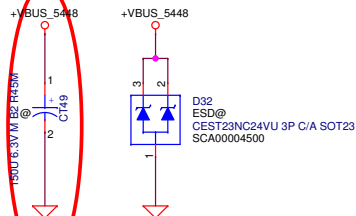
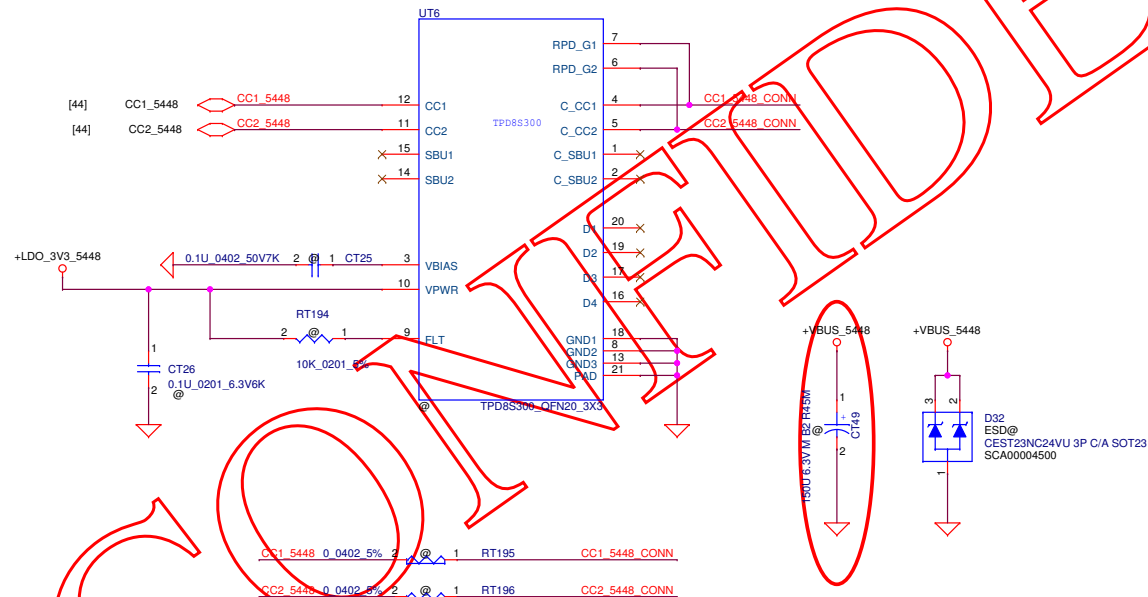
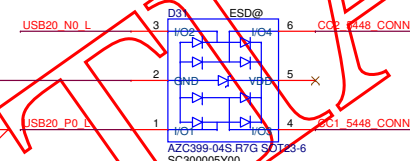
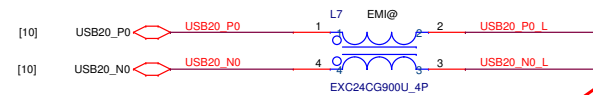
Power switch enable pin	Note
Low Active	RT188/RT185 mount
High Active	RT188 mount, RT185 don't mount
Power switch OCP pin	Note
Low Active	RT189/RT186 mount
High Active	RT189 mount, RT186 don't mount

DRAPH_UB11245-B200B-1H_24P-S change to -T



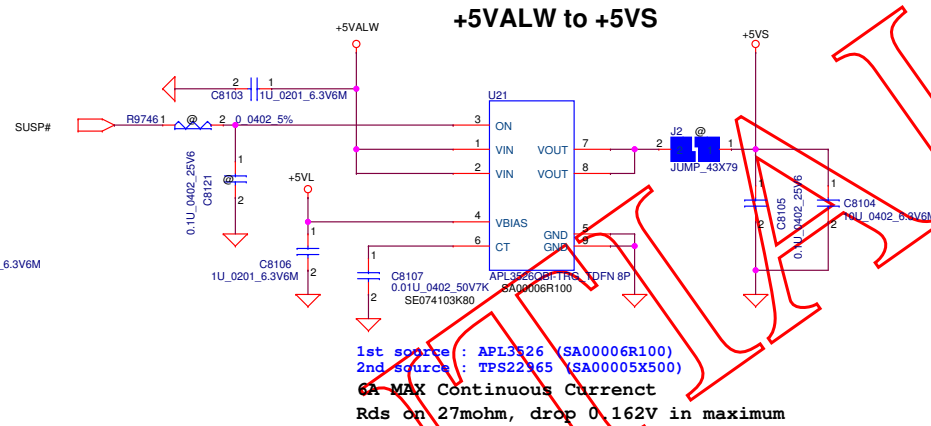
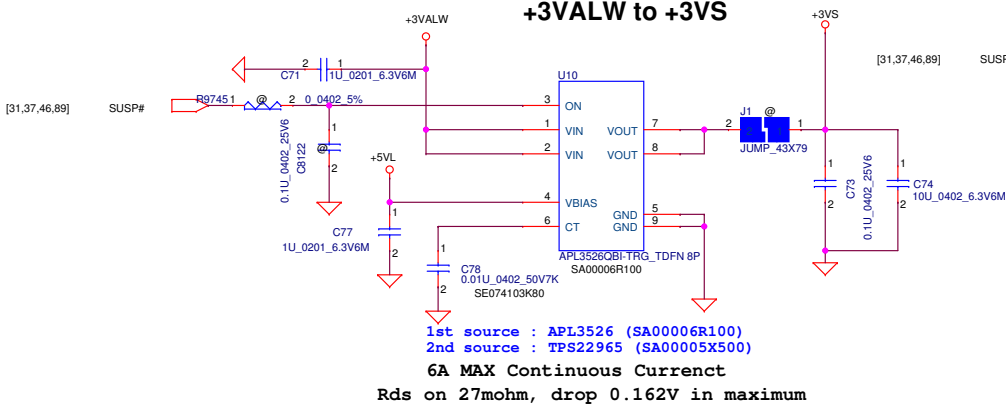
CONN FROM Y750

Type-C Connector PN
TMP DC231703291

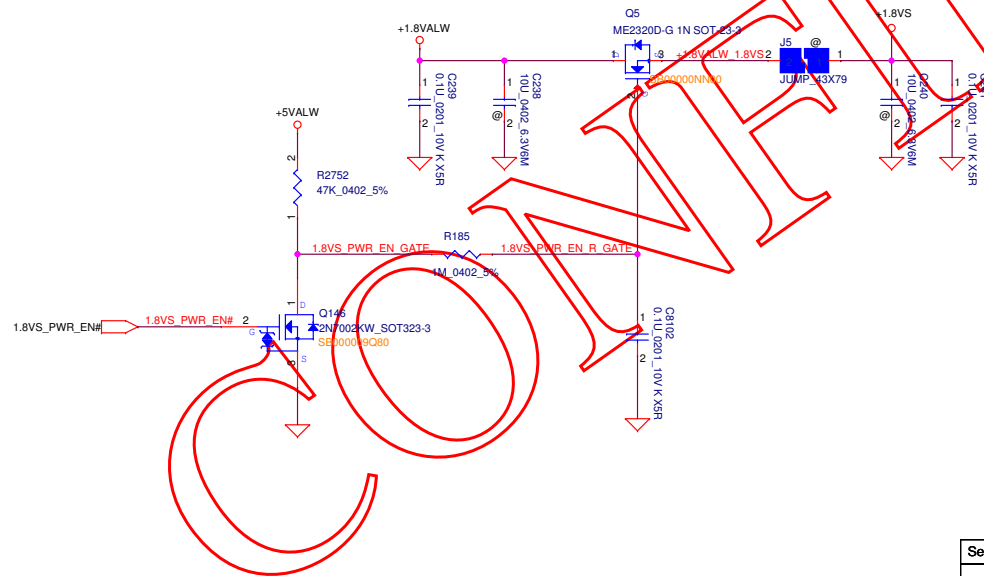


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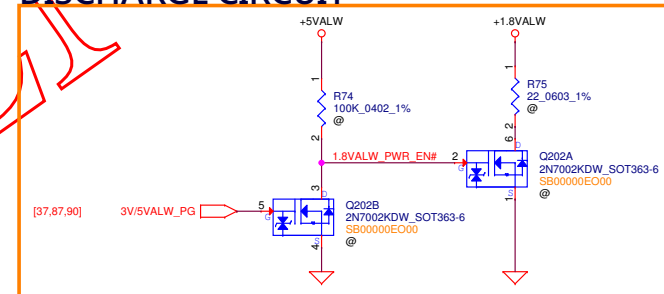
DC to DC



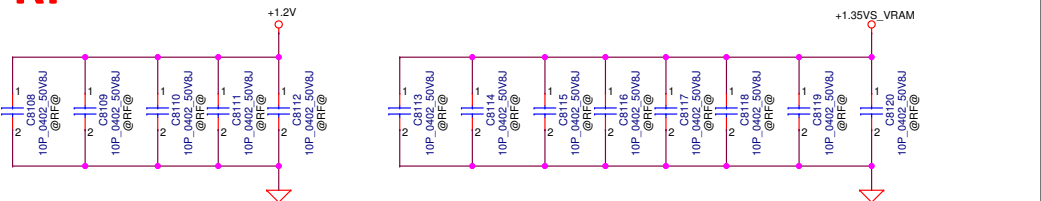
+1.8VALW to +1.8VS / +0.75VALW to +0.75VS



DISCHARGE CIRCUIT



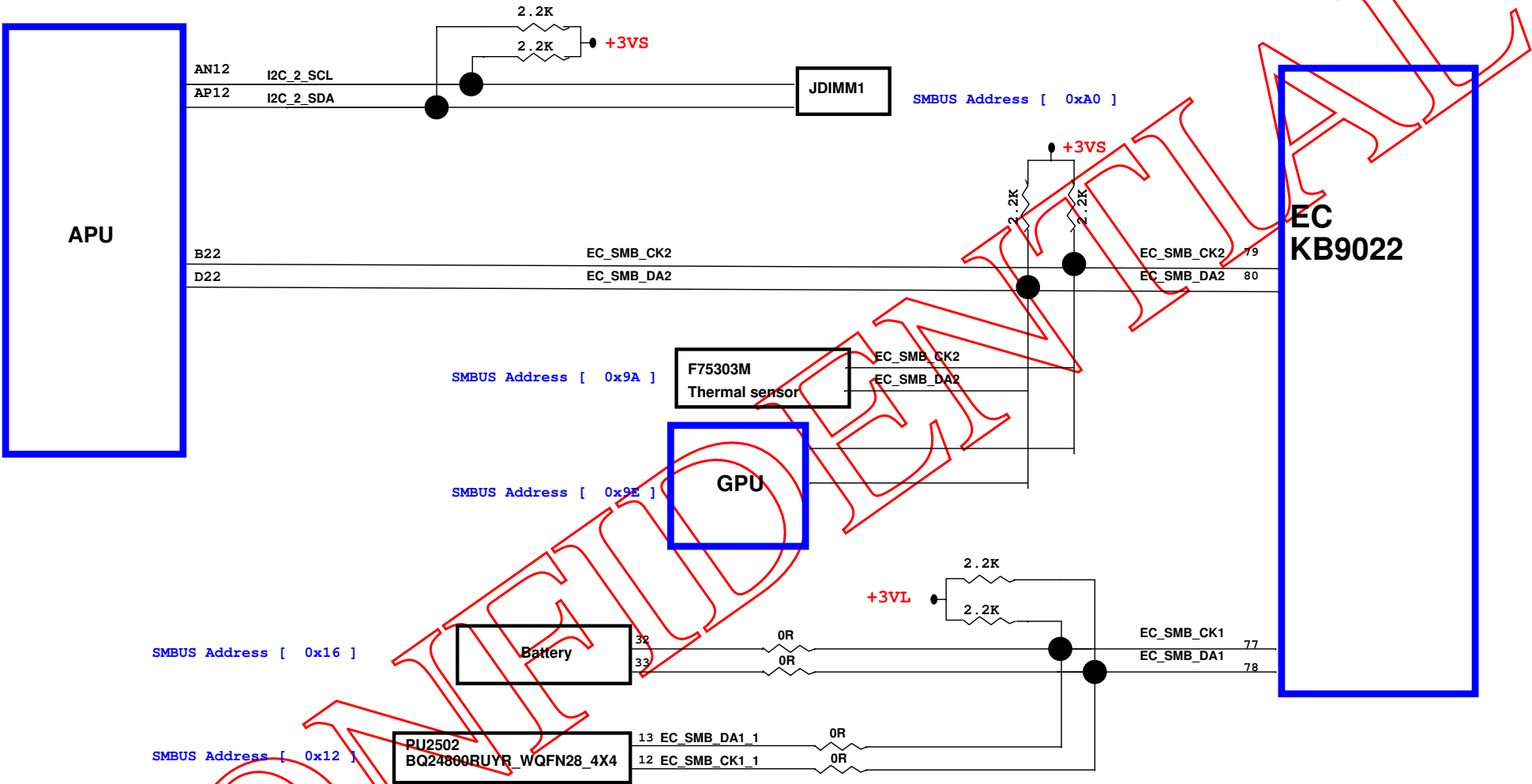
RF



+1.8VALW Discharge Circuit (Reserved)

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SMBus Block Diagram



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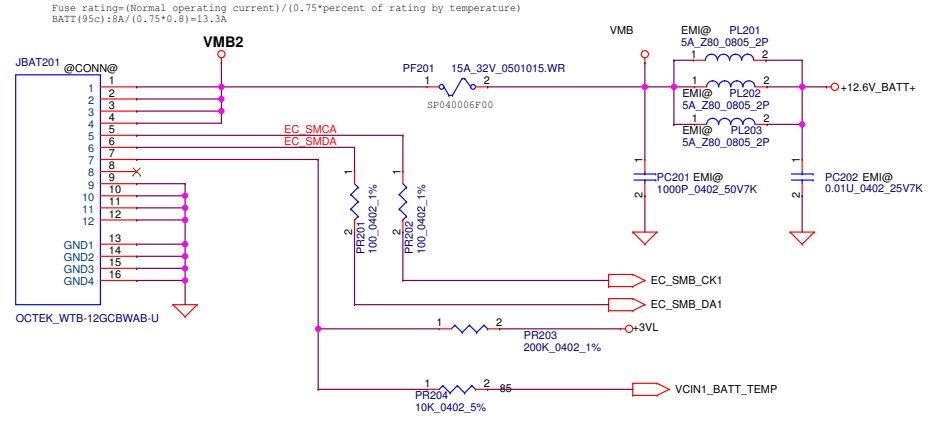
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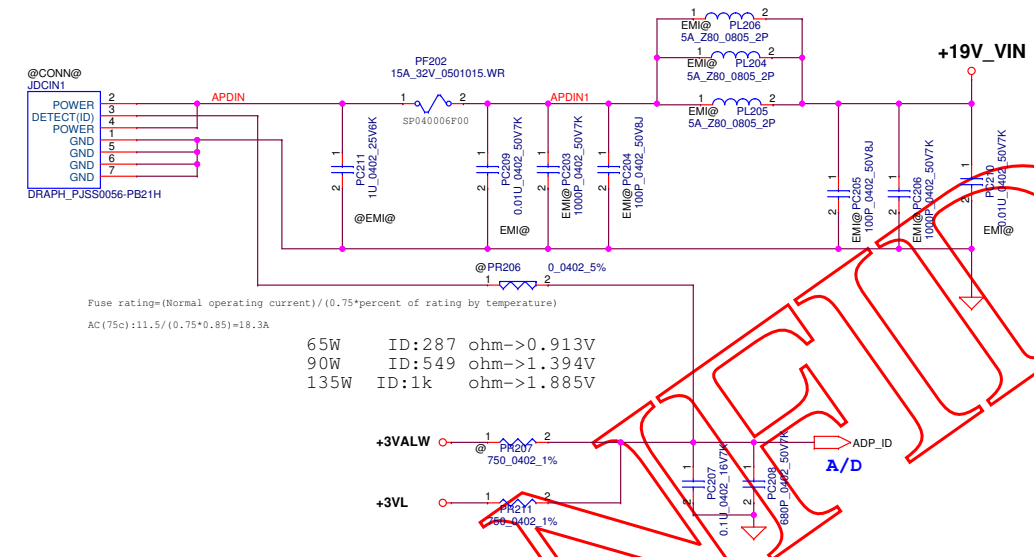
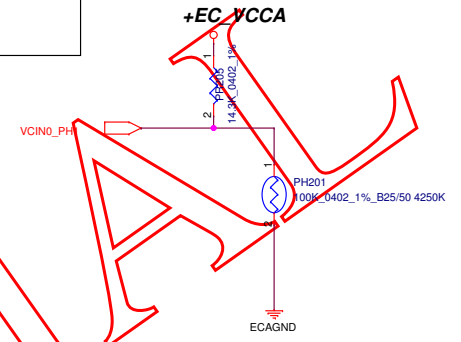
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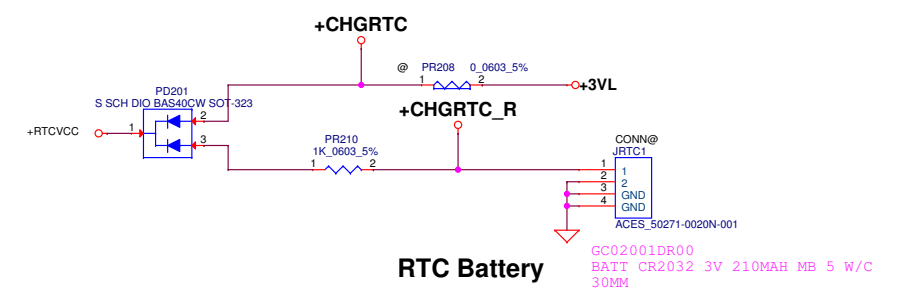


PH201 under CPU bottom side :
CPU thermal protection at 97 +-3 degree C
Recovery at 59 +-3 degree C



Fuse rating=(Normal operating current)/(0.75*percent of rating by temperature)
AC(75c):11.5/(0.75*0.85)=18.3A

65W ID:287 ohm->0.913V
90W ID:549 ohm->1.394V
135W ID:1k ohm->1.885V



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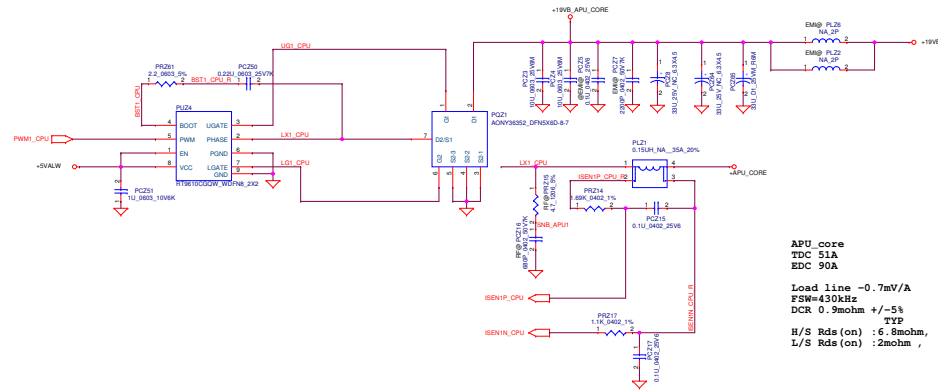
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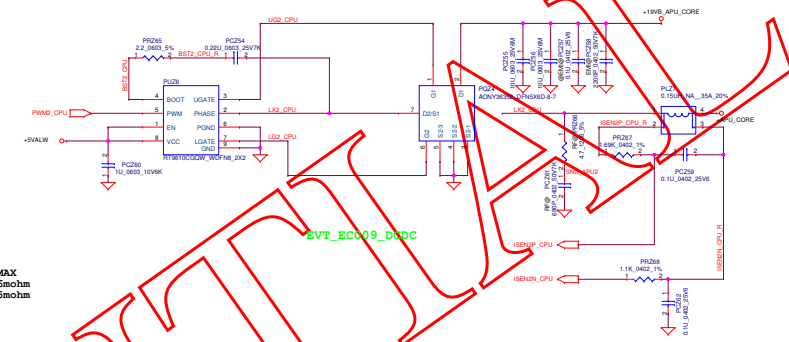


Vcore
L=0.15uH, DCR=0.9mohm, LL=0.7mohm, EDC=110A, OCP=EDC*1.4=154A
Vcore_NB
L=0.22uH, DCR=4.3mohm, LL=2.1mohm, EDC=20A, OCP= EDC*1.4=28A

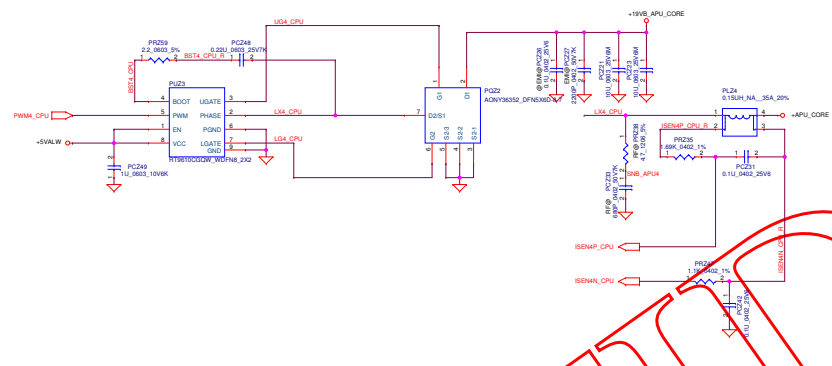
SDV_EC004_DCDC



EVT_EC009_DCDC

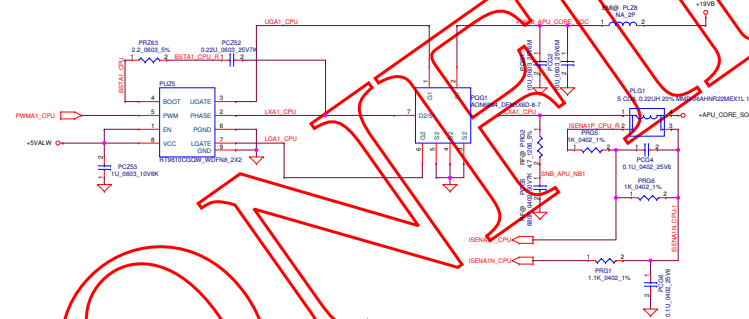


EVT_EC009_DCDC



APU_CORE_SOC
TDC 15A
EDC 20A

Load line -2.1mV/A
FSW=400kHz
DCR 1.19mohm $\pm 5\%$
H/S Rds (on) : 6.8mohm, 8.6mohm
L/S Rds (on) : 2mohm, 2.5mohm



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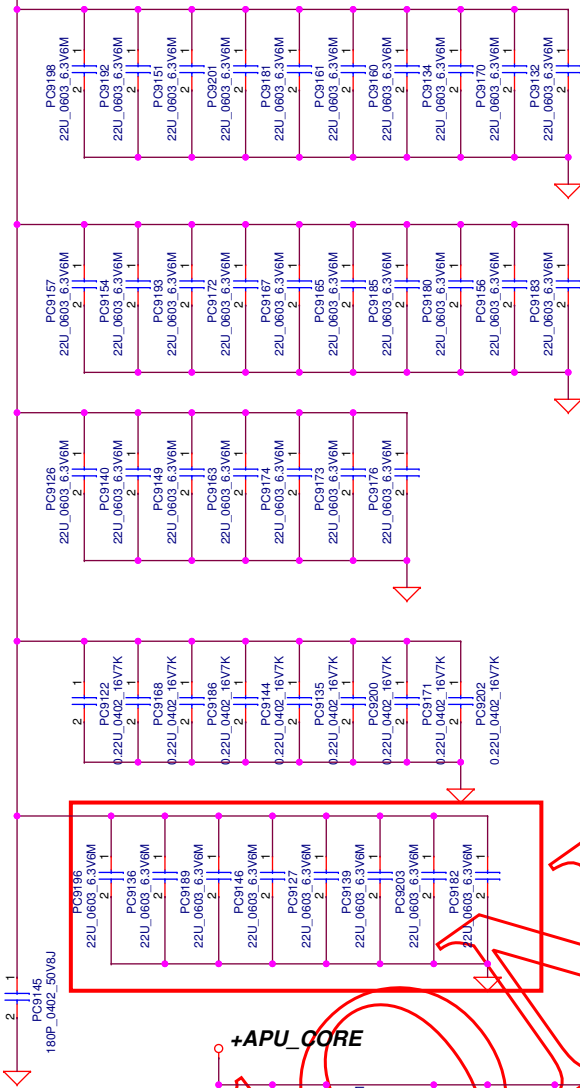
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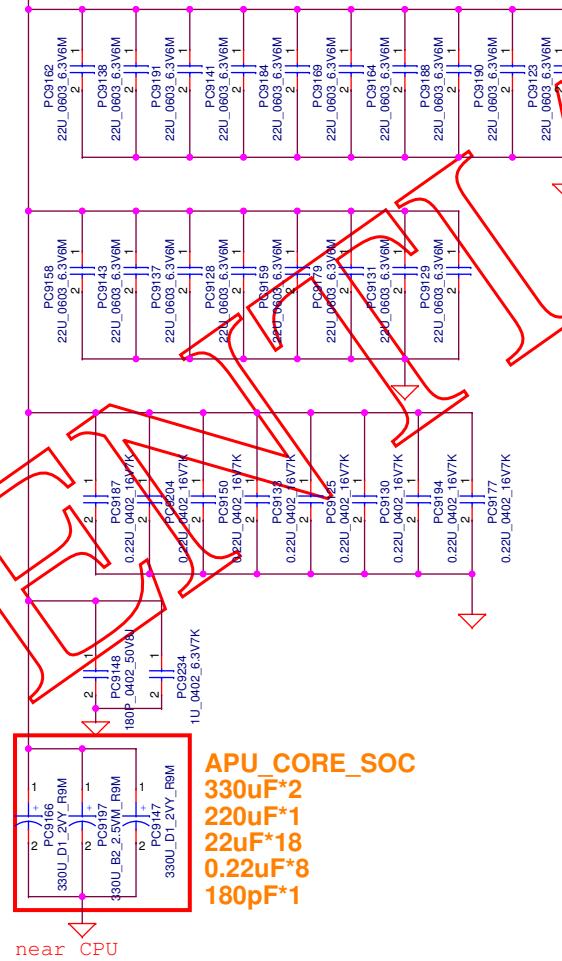
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+APU_CORE_SOC

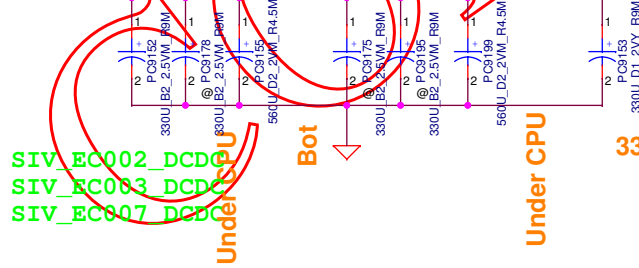
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+APU_CORE_SOC

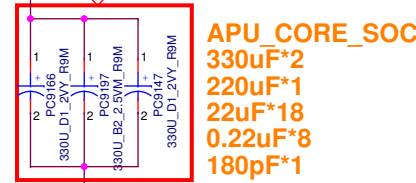


+APU_CORE



APU CORE
330uF*5 220uF *4
22uF*27
0.22uF*8
180pF*1

330u is common part SGA00009S00



near CPU
330u is common part SGA00009S00

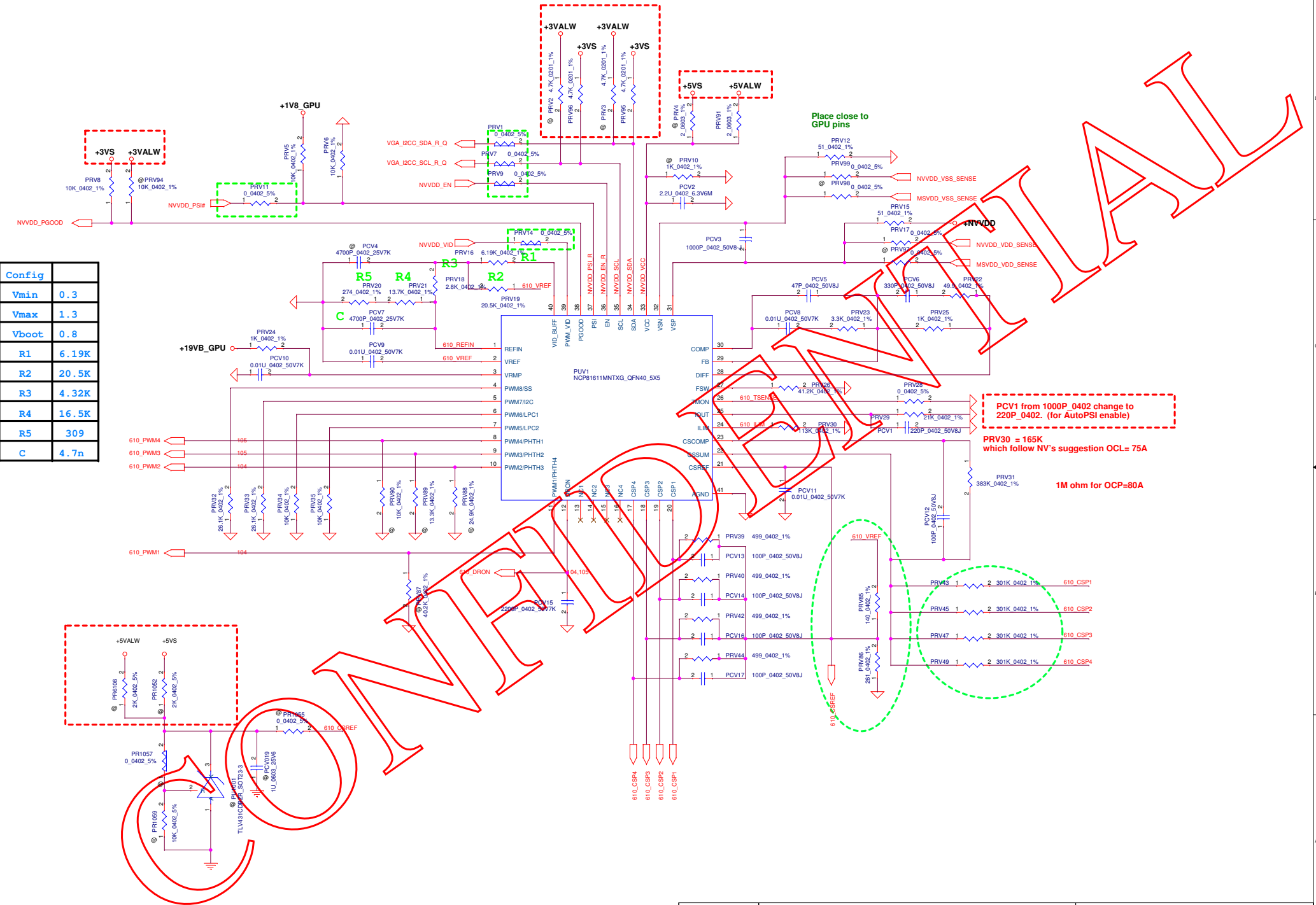
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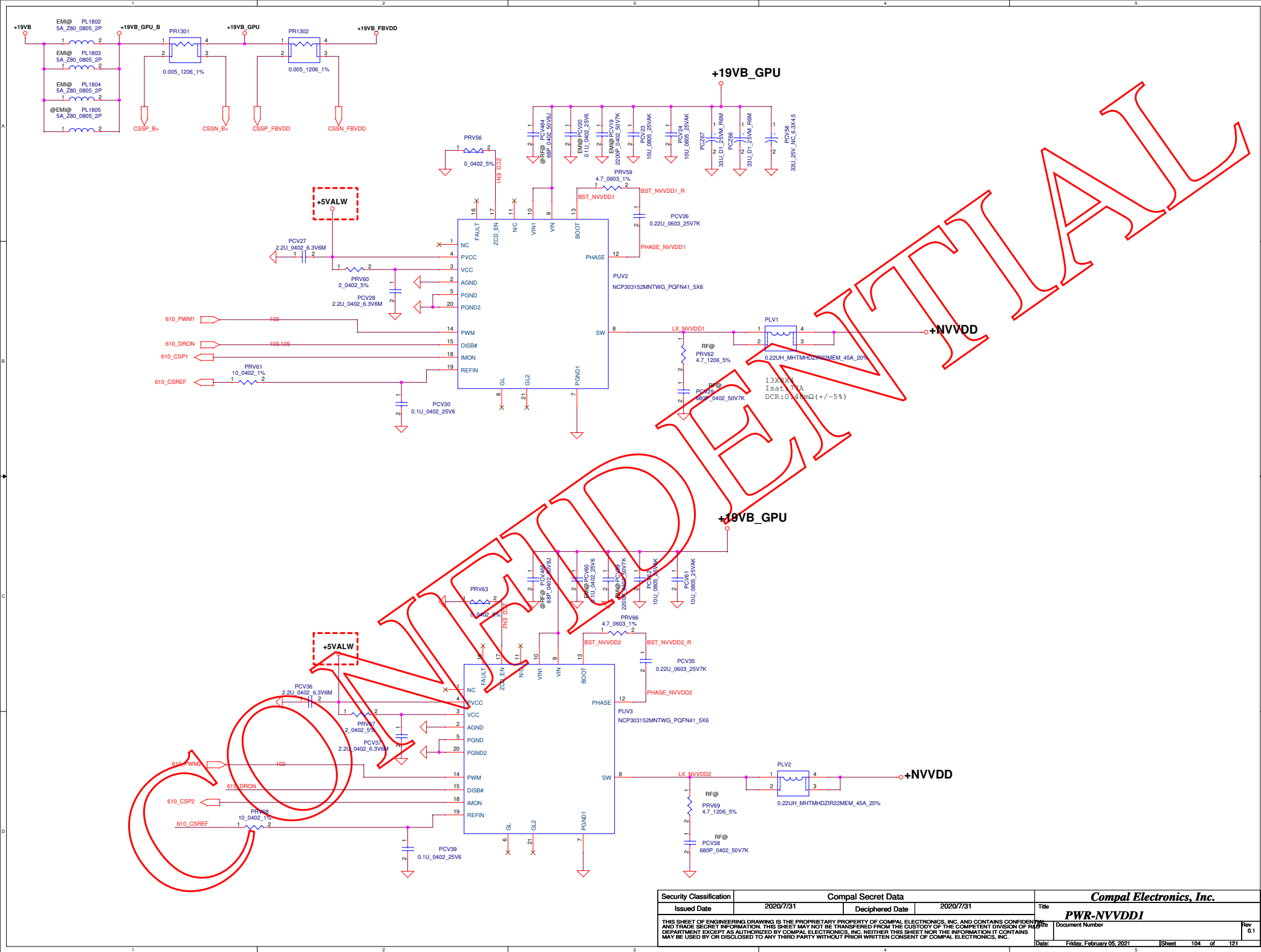
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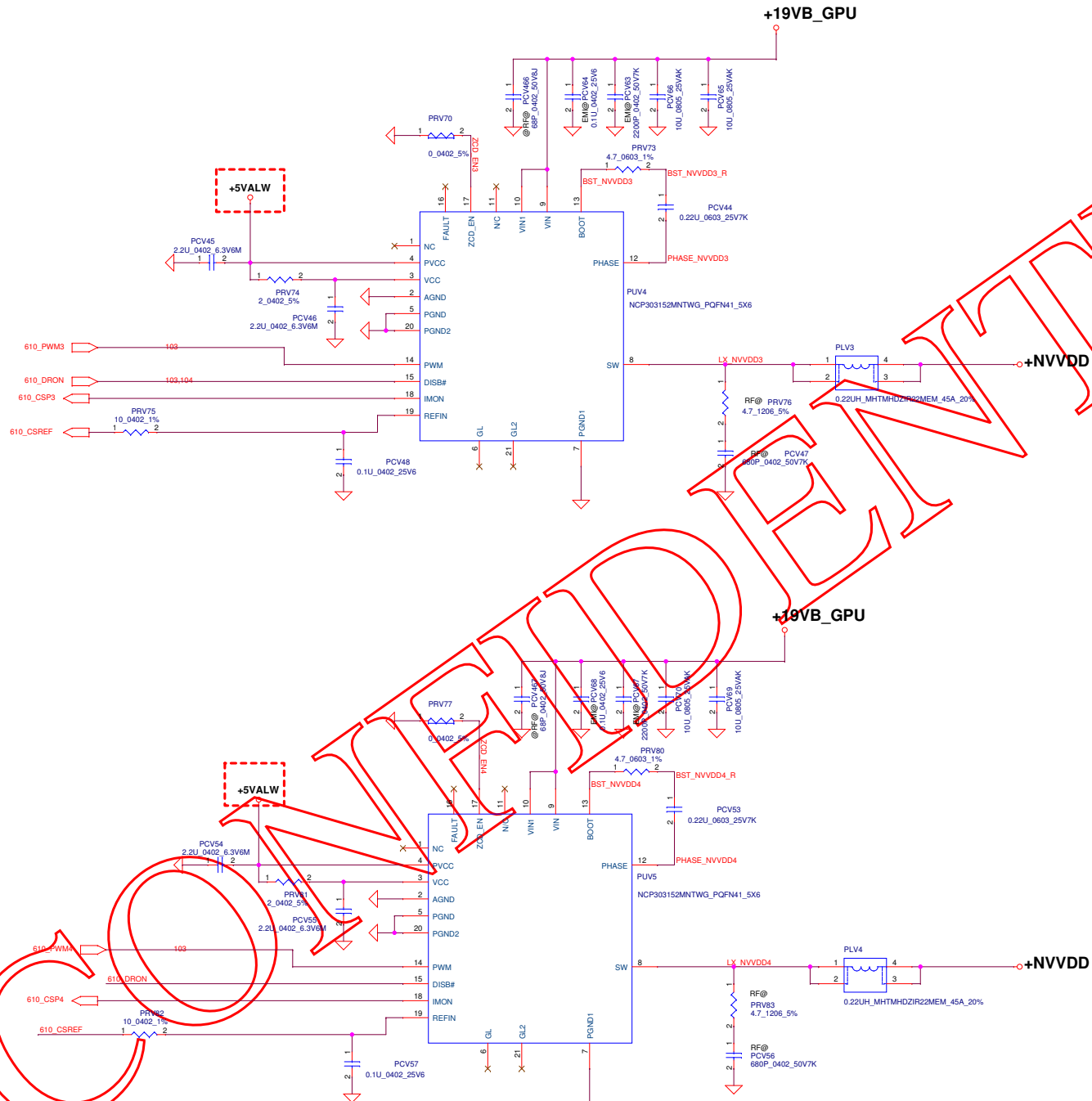
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Config	
Vmin	0.3
Vmax	1.3
Vboot	0.8
R1	6.19K
R2	20.5K
R3	4.32K
R4	16.5K
R5	309
C	4.7n







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Samsung & Micron VRAM
When, VRAM_VDD_CTL=High
Vboot=1.25V
When, VRAM_VDD_CTL=Low
Vboot=1.2V

PSI=0.79V
When the voltage is
between 0.7V to 0.88V,
the device will operate into
1 phase force CCM

MOSFET: DFN 5X6E
H/S Rds(on) : 5.2mohm(Typ), 7mohm(Max)
L/S Rds(on) : 0.8mohm(Typ), 1.05mohm(Max)

+19VB_FBVDD

+1.35VSDGPU
M18P-G62
TDC 17.2A
Peak Current 18.4A
OCP current 30A
fsw=400kHz

+1.35VS_VRAM

$OCP = [(10\mu A * 76.8k) / (12 / 1.8m) + (5A / 2)] * 1\text{phase} = 38A$

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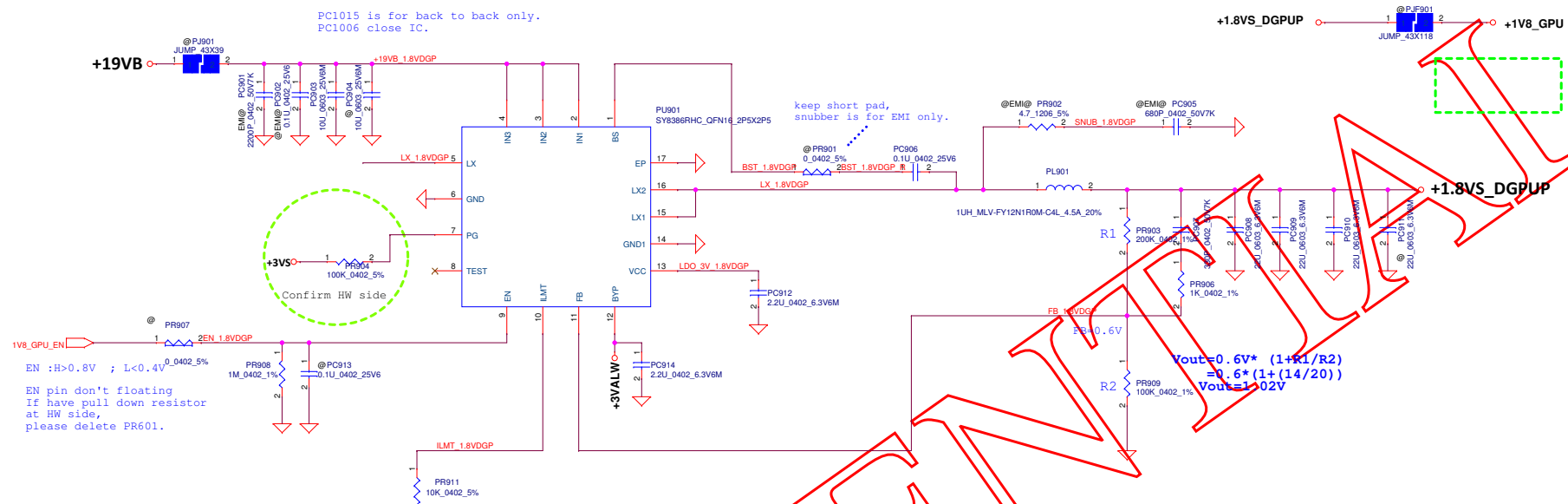
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Module model information

SY8386_V1.mdd

PC1015 is for back to back only.
PC1006 close IC.

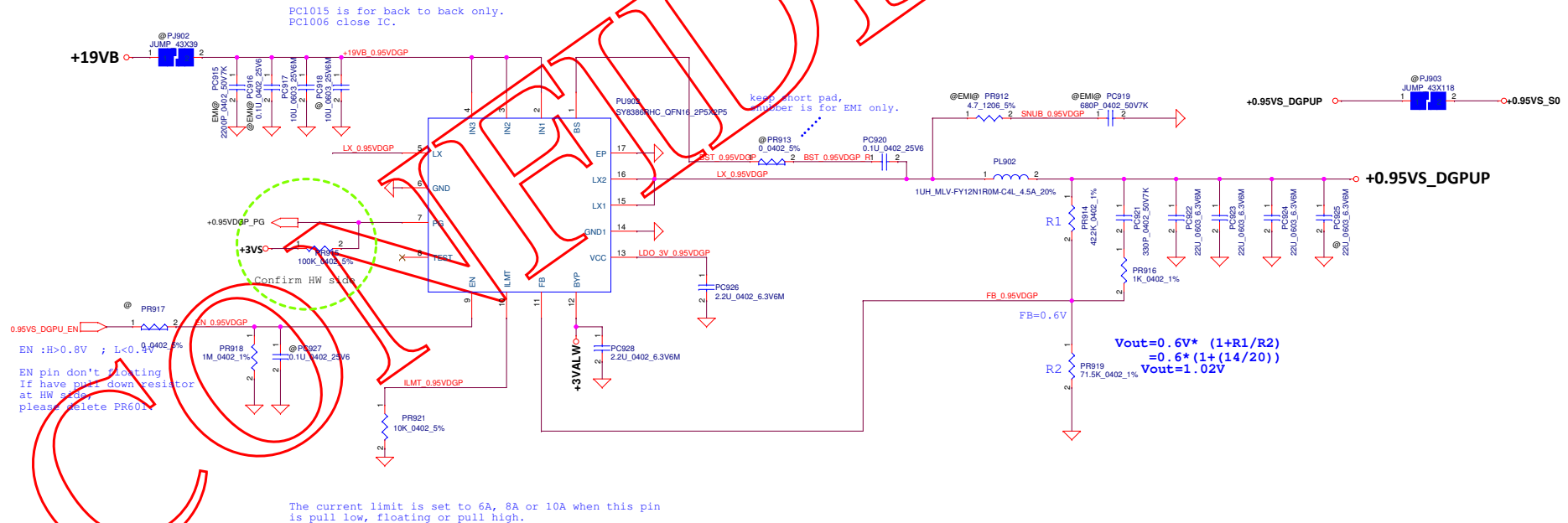


Module model information

SY8386_V1.mdd

The current limit is set to 6A, 8A or 10A when this pin is pull low, floating or pull high.

PC1015 is for back to back only.
PC1006 close IC.



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Item	Reason for change	PG#	Modify List	Date	Phase
1	Design circuit for battery FW	85	ADD PQ311,PR335,PR336,PR338,PC9231	2020/11/03	
2	Change choke for common design	85	PL2503 4.7uH -> 2.2uH		
3	Remove charger IC DH_CHG resistance	85	PR316 1/10W 0 --5% 0603		
4	Remove -3V1 to F6 resistance	90	PR1812 1/16W 100K --5% 0402		
5	Remove GPU_VRAM_Cap	108	PCW24, PCW25 22U 6.3V M X5R 0603	2020/11/20	
6	update GPU_CORE_Phase location &Remove	107	47u 6.3V cap All location update &Remove 2 cap		
7	change Bulk for COMMON design	107	PCW12 330u 2V --560u 2V PCV467,PCV468,PCV469,PCV470,PCV471 330u 2V --PC1001,PC1002,PC1003,PC1004,PC1005 560u 2V		
8	Remove APU_CORE_DECOUPLING Bulk	101	PC9142 330u 2.5V		
9	ADD GPU_CORE_Phase Bulk	107	PC1173 330u 2V		
10	change APU_CORE_DECOUPLING Bulk	101	PC9155,PC9199 220U 2V --> 330U 2V		
11	Remove GPU_CORE_Phase Bulk	107	PCV472 220U 2V		
12	Change choke for common design	98	PL61 0.22uH --20% 24A -->0.22uH 20% 14A		
13	Change choke for common design	98	PLZ1,PLZ4,PLZ5,PLZ7 0.15uH --20% 36A --> 0.15uH --20% 35A		
14	ADD charger ACIN_thermisto	85	PH301 10K_0402_50%_TPM06103P130R		
15	ADD GPU_CORE Bulk TO -NVVDD	107	PC1000 560U_D2_2VM_R4.5M *1		
16	ADD APU_CORE_SOC resistance	98	PR66 SRES 1/16W 1K --1% 0402	2020/11/06	
17	Change resistance for common design	98	PR65 SRES 1/16W 2K --1% 0403 --> SRES 1/16W 1K --1% 0403	2020/11/16	
18	Change resistance for common design	99	PR61 S RES 1/16W 845 --1% 0402-->S RES 1/16W 1.1K --1% 0402		
19	Change resistance for common design	97	PR61813 S RES 1/16W 16.9K --1% 0402-->S RES 1/16W 10K --1% 0403		
20	Change resistance for common design	97	PR6118 S RES 1/16W 18K --1% 0402-->S RES 1/16W 15.4K --1% 0402		
21	Change JUMP for common design	110	*PJ302 JUMP 43*79 -->43*39		
22					
23	Change resistance for common design	97	PR1808 S RES 1/16W 8.45K --1% 0402-->S RES 1/16W 11K --1% 0403	2020/11/17	
	Change MLCC for common design	85	PC9213 0.01u -->0.1u		
	Change MLCC for common design	87	PC519 1000P -->470P		
25	Add resistance for common design	108	PRW136 0 Ohm		
26	Add Bulk for common design	107	PC9232 --PC9233 47u		
27	Change resistance for common design	85	PR350 ,PR351 1K --> 0hm		
28	Change resistance for common design	97	PR1813 10K -->75.7 PR6118 15.4K -->14.3K PR1808 11K-->12.1K PR1807 88.7K -->76.8K		
30	Add resistance for common design	103	PRV91,		
31	Remove resistance for common design	103	PRV4'		
32	Change Short pad for common design	89	PR2503		
33	Change Short pad for common design	97	PR1829 PR1855 PR6115 PR6116 PR6117 PR1817 PR1852 PR1855 PR1814 PR1829		
34	Change Short pad for common design	103	PRV11 PRV28		
	Add resistance for common design	103	PRV91		
35	Add resistance for common design	108	PRW135		
36	Add MLCC for common design	85	PC9228 PC9229		
37	Remove resistance for common design	103	PRV87 PRV88 PRV89 PRV90		
38	Change Bulk Size for common design	104	PC9166		
39	Add sensor for common design	85	PH301		
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